

## SECTION 8—ELECTRONICS TECHNOLOGY

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### *Highlights*

- Moore's Law, which states that the number of transistors per chip will double every 18 months, continues to drive the electronic evolution and will enable smaller size, lower power, higher reliability, and lower cost electronics. However, the electronic materials and manufacturing technologies must be advanced to allow this rapid progress to take place, and this advance will be very costly.
- Nanoelectronics (below 100 nm) will be the successor to microelectronics but will require much research and development (R&D) in all areas since a paradigm shift in physics, materials, and processing is required.
- Microwave and other radio frequency (RF) components continue to progress, with increased power and frequency capability and reduced size and weight.

### **OVERVIEW**

This section discusses the general-purpose integrated circuit (GPIC) devices and the materials and processes, software, test, and packaging technologies required to produce and maintain the finished product. These circuits can be digital, analog, hybrid digital and analog, analog-to-digital (A/D), and digital-to-analog (D/A) converters, microwave, and optical and optoelectronic if integrated on a GPIC or a module (see Section 11.5 for optoelectronics).

Also included are:

- General-purpose modules made of these devices if packaged as multi-chip modules (MCMs) or printed circuit boards (PCBs)
- Other combinations of optical, microelectromechanical systems (MEMS), or micromachines used as sensors, effectors, input, output, or internal processing functions resulting in a "system-on-a-chip"
- Microwave components, vacuum tubes [e.g., traveling wave tubes (TWTs)] and their constituent parts
- General-purpose electronic equipment (e.g., test equipment, tape recorders, and their media and other general-purpose structures).

The electronic materials and fabrication technologies covered are unique to electronic manufacture and generally operate at the submicron dimension for electronics. One exception is the MEMS area, which produces devices at the multiple micro to submicron dimension using the same technology described in this section and which can be integrated into devices containing MEMS, electronic, and optical technologies. Other machine technologies can be found in Section 12, Manufacturing and Fabrication Technology.

The general trend of these technologies is to create rapidly the higher performance, smaller size, lower power, higher reliability, and greater integrated functionality necessary to perform a wide range of applications. The use of these products is pervasive across all applications, both commercial and military. The commercial sector is the pri-

mary driver and market for these products. However, the military sector has the same requirements for high performance, small size, lower power, and integrated functionality and has a greater requirement for reliability, temperature range, and radiation-hardened (rad-hard) characteristics. The technologies involved in these products result in increasingly higher reliability and rad-tolerant devices because of the materials and processes involved.

The major force driving the electronics technologies is the goal of increasing the density of devices, with improvements in all the other characteristics noted previously and generally adhering to “Moore’s Law,” which anticipates halving device size every 3 years. For instance, the goal stated in the Semiconductor Industry Association (SIA) National Technology Roadmap for Semiconductors (NTRS) for the year 2000 is 250 to 150 nm for production chips. These dimensions are pushing the present optical lithography technologies to their limit. Extreme ultraviolet (EUV) lithography will help continue the reduction in feature size (see Section 8.3). However, attaining the next two generation goals of reduction to less than 100 nm will require a new paradigm of electronic technologies where Moore’s Law may not apply. The new physics and the new fabrication processes necessary to reach this “nanoelectronic” capability are a huge challenge for the next century (see Section 8.5).

As noted, commercial industry is the driving force for many advances in electronics technology—pushing lightweight, smaller size, and lower power devices as far as possible for laptop computers, handheld devices, and so forth. However, the military has the same goals for “personal wearable electronics,” land-vehicle electronics, ultralightweight and unmanned surveillance aircraft for “the battlefield of the future,” ocean applications (e.g., smart mines), and space electronics. Many of these military applications require even lower power, smaller size, and higher reliability than any commercial application.

## ***RATIONALE***

Electronics are pervasive across all military systems and dramatically improve system performance. This continual improvement in the electronics performance gives the United States a distinct advantage in the military arena. High-performance electronics are used in strategic and tactical air, ground, surface and underwater, and space applications. The parameters of small size, low weight, low power, high reliability, and affordability give modern electronics systems their superiority.

Almost all the advances in electronic technology, particularly microelectronics, are made in the commercial arena. The large costs involved in the fabrication of microelectronics prohibit the military from pursuing technology development in these areas, except in rare instances. However, the military is moving to use commercial electronics directly through the commercial-off-the-shelf (COTS) program. The COTS option is possible because advances in electronics inherently make electronic devices more immune to environmental characteristics, such as temperature, shock, vibration, and radiation. Increasing miniaturization toward system-on-a-chip reduces overall off-chip connections, PCBs, and so forth while reducing size and weight, thereby reducing susceptibility to shock and vibration.

## ***TECHNOLOGY ASSESSMENT***

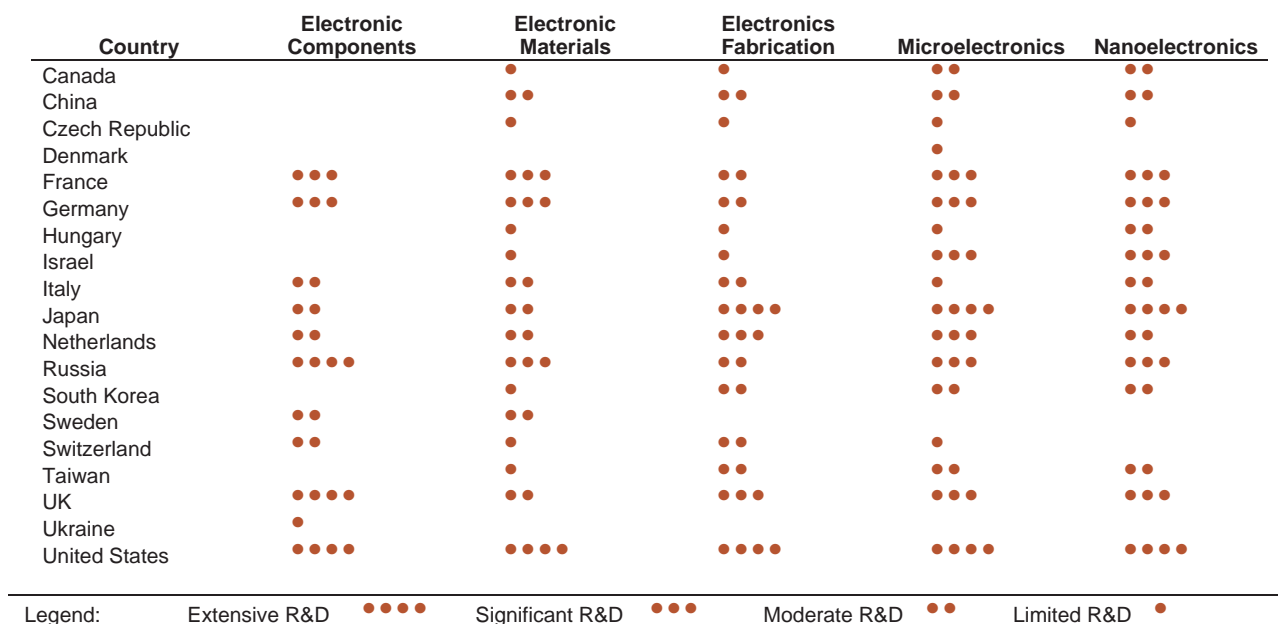
Commercial products (e.g., high-performance computers and microprocessors; handheld portable electronics general-purpose computer devices; very small portable telephones; and small, high-performance but low-power electronics) will continue to define the electronics technology. The 1997 SIA NTRS defines the future expectations for the semiconductor industry to the year 2012. They expect that semiconductor feature size will be 50 nm by that time; however, the roadmap timing has recently slipped several years because of more than excess effort to achieve the next-generation fabrication technology. In addition, the expectation of reaching 50 nm in 2012 was very optimistic since passing the region between 150 nm and 200 nm is a stretch for present fabrication. Reaching sizes below 100 nm requires a complete paradigm shift in all aspects of the device physics and in cost-effective fabricating techniques. Sections 8.2, 8.3, and 8.5 detail these technologies.

The SIA NTRS predicts the production of 4-GB memories and the sample introduction of 16-GB memories by the year 2006. Also at that time, it predicts 40 million gates per chip in microprocessors. One might ask, when does the need saturate and is there less utility in further increases in density? The answer so far is that the market has been completely elastic and all performance improvements have been absorbed by the products offered to the consumer. As the new century gets underway, a large increase is expected in the integration of electronics, MEMS, and optoelectronic components. This integration has been named “system-on-a-chip.” Of course, lower level integration of

digital, analog, and hybrid electronics has been occurring and will continue to accelerate. Integration of optical and electronic components on a chip is described in Section 8.5, Microelectronics.

Continual development in satellite communications requires better technology in vacuum tubes and RF components, and the improved miniaturization, power, frequency, and reliability of millimeter-wave (mmW) components are required to maintain superiority in all the “information” technologies (see Section 11.3). Intelligence gathering requires improved recording technology, such as optical tape recorders and media (see Section 8.4).

**WORLDWIDE TECHNOLOGY ASSESSMENT** (see Figure 8.0-1)



**Figure 8.0-1. Electronics Technology WTA Summary**



## SECTION 8.1—ELECTRONIC COMPONENTS/MICROWAVE TUBES

### *Highlights*

- Microwave power modules (MPMs) offer increased power and frequency capability, with reduced size and weight.
- Improved cathodes with lower work functions will result in microwave tubes that can operate with greater efficiency, higher current density, and longer cathode life.
- Overall improvements in TWT technology will result in TWTs capable of operating in the kW power range, at frequencies greater than 90 GHz.

### **OVERVIEW**

This section addresses developing technologies in the field of high-power microwave components, with particular application in surveillance, satellite communications, electronic warfare (EW), missile seekers, and tracking radar. These modern weapons require high levels of microwave power, and semiconductors are presently not suitable for these high-power applications. Although development of SiC semiconductor devices may alleviate this shortcoming, microwave tubes are presently the most effective devices for these applications.

Efforts to enhance the performance of these microwave components include improving each of the inherent parts of conventional TWTs (including the cathode), improving the cooling of the RF section (particularly in helix tubes), improving the ability of the electron beam to focus, and combining the technologies of TWTs with solid-state devices to form assemblies called MPMs. Research to improve the cathodes includes efforts on thermionic and nonthermionic cathodes, specifically developing new coating materials to extend the life of the cathodes and their current densities and evaluating the use of field-emission cathode arrays (cold cathodes). Improved cooling of the TWT has a significant effect on the power handling of the tube, and studies are being performed on the effect of substituting diamond-coated rods, with their superior thermal conductivity, for the more conventional support rods used in helix tubes. Focusing is a critical aspect of tube design and manufacture since energy that falls on (is absorbed by) the RF structure decreases the efficiency of the tube. Studies are also underway to develop stronger and more reliable magnets to minimize the “stray energy,” thus improving the efficiency of the TWTs.

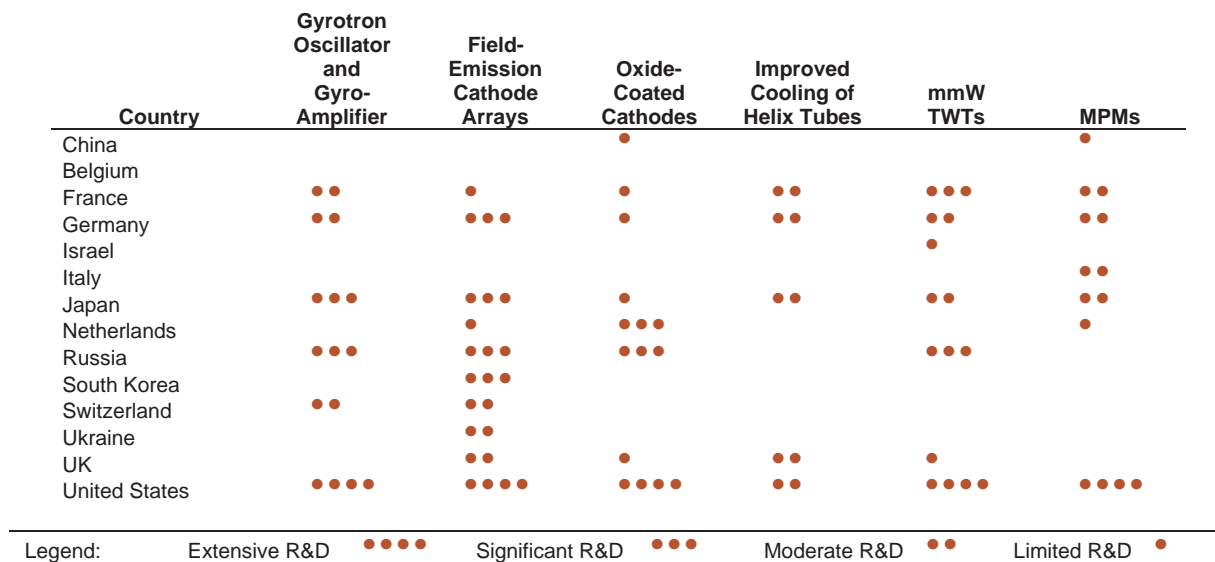
MPMs combine several technologies: mmW integrated circuits (MMICs) for amplification, helix TWTs for power amplification, and an electronic power conditioner (EPC). This combination of technologies provides optimum use of each of the technologies: frequency amplification by the MMICs and power amplification by the TWTs.

### **RATIONALE**

Microwave components are used in military ground, ship, missile, and airborne applications. This includes radar, fire control, EW, decoys, missile seekers, and communications. Radar, fire control, and EW have an increasing need for all-weather, high-performance systems capable of penetrating obscurants to achieve target detection. To accomplish these tasks, devices that have power levels of greater than 10 kW, frequencies greater than 30 GHz, and wide bandwidths must be developed.

Satellite communications, whether military or civil, are dependent on the power, frequency, and reliability of mmW components. Improvements related to these parameters are essential in developing and maintaining the “information superiority” described in Joint Vision 2010. Miniaturization of mmW components is necessary in decoys, missiles (and missile seekers), and unmanned aerial vehicles (UAVs). MPMs with improved capabilities will be used even more in these applications.

**WORLDWIDE TECHNOLOGY ASSESSMENT** (see Figure 8.1-1)



**Figure 8.1-1. Electronic Components/Microwave Tubes WTA Summary**

**LIST OF TECHNOLOGY DATA SHEETS**  
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Improved Cathodes: Field-Emission Cathode Arrays (Cold Cathodes) .....	III-8-10
Improved Cathodes: Oxide-Coated Cathodes .....	III-8-11
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Millimeter-Wave (mmW) Traveling Wave Tubes (TWTs) .....	III-8-13
Microwave Power Modules (MPMs) .....	III-8-14





### DATA SHEET III-8.1. GYROTRON OSCILLATOR AND GYRO-AMPLIFIER

<b>Developing Critical Technology Parameter</b>	Continuous wave (CW) power greater than 5 MW and a frequency greater than 30 GHz.
<b>Critical Materials</b>	Superconducting coils; exit window material.
<b>Unique Test, Production, Inspection Equipment</b>	None identified.
<b>Unique Software</b>	None identified.
<b>Technical Issues</b>	Magnetic properties; mirror; optical window capable of handling the RF power.
<b>Major Commercial Applications</b>	Fusion research; thermal processing of materials (ceramic sintering and welding); driving linear colliders.
<b>Affordability</b>	Not an issue.

#### ***RATIONALE***

Gyrotron oscillators have opened up the mmW region (1-to-10 mm) for high-power applications. Present gyro-devices are capable of operating at continuous power levels approaching 1 MW at frequencies exceeding 100 GHz. Present gyro-amplifiers (e.g., gyro-klystrons) are capable of operating at average power levels of 10 kW over a 1-GHz bandwidth at a center frequency of 94 GHz. Military applications are mmW radar (e.g., fire control radar and tracking radar for targets close to the sea surface).

#### ***WORLDWIDE TECHNOLOGY ASSESSMENT***

France	• • •	Germany	• •	Japan	• • •	Russia	• • •
Switzerland	• •	United States	• • • •				

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Legend:      Extensive R&D    • • • •      Significant R&D    • • •      Moderate R&D    • •      Limited R&D    •

### DATA SHEET III-8.1. IMPROVED CATHODES: FIELD-EMISSION CATHODE ARRAYS (COLD CATHODES)

<b>Developing Critical Technology Parameter</b>	Current densities of 1,000 to 2,000 A/cm <sup>2</sup> .
<b>Critical Materials</b>	Silicon; diamond (carbon); GaN; other materials being researched to form field emission tips.
<b>Unique Test, Production, Inspection Equipment</b>	Photolithographic equipment; plasma etchers; and so forth.
<b>Unique Software</b>	Computer-aided design/computer-aided manufacturing (CAD/CAM).
<b>Technical Issues</b>	Developing a material with an improved lifetime of the tips in the cathode array.
<b>Major Commercial Applications</b>	Space electronics; radar systems; flat panel displays (FPDs).
<b>Affordability</b>	Not an issue.

#### ***RATIONALE***

Field-emission cathode arrays hold great promise for improving microwave devices. They should provide much greater current densities (and, thus, greater output power) than more conventional heated cathodes and do not require external heaters. Thus, TWTs using this type of cathode could not only produce greater power, but, because of the absence of heaters, produce this power in a smaller device envelope.

#### ***WORLDWIDE TECHNOLOGY ASSESSMENT***

France	•	Germany	•••	Japan	•••	Netherlands	•
Russia	•••	South Korea	•••	Switzerland	••	Ukraine	••
UK	••	United States	••••				

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Legend:      Extensive R&D    ••••      Significant R&D    •••      Moderate R&D    ••      Limited R&D    •

### DATA SHEET III-8.1. IMPROVED CATHODES: OXIDE-COATED CATHODES

<b>Developing Critical Technology Parameter</b>	Reduce work function from 2.0 eV to 1.2 eV.
<b>Critical Materials</b>	Oxide-coated cathodes: barium and strontium oxides, scandate ( $\text{Sc}_2\text{O}_3$ ); indium and scandium oxides; and indium as an additive; impregnated cathodes; lanthium hex-aboride cathodes.
<b>Unique Test, Production, Inspection Equipment</b>	Deposition techniques (usually plasma deposition); pulsed laser deposition.
<b>Unique Software</b>	None identified.
<b>Technical Issues</b>	Coating composition and uniformity; avoiding cathode poisoning.
<b>Major Commercial Applications</b>	Space electronics and radar systems.
<b>Affordability</b>	Not an issue.

#### ***RATIONALE***

By developing cathodes with lower work functions, microwave tubes can operate with greater efficiency (i.e., greater output power at the same level of dissipated heat) and higher current density and enjoy longer cathode life. These improvements would be of value for a range of microwave tubes, TWTs, magnetrons, and so forth.

Improvements in these tubes will have considerable effect on military electronics, including radar, EW, and space electronics.

#### ***WORLDWIDE TECHNOLOGY ASSESSMENT***

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Netherlands	• • •	Russia	• • •	UK	•	United States	• • • •

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Legend:      Extensive R&D    • • • •      Significant R&D    • • •      Moderate R&D    • •      Limited R&D    •

### DATA SHEET III-8.1. IMPROVED COOLING OF HELIX TUBES

<b>Developing Critical Technology Parameter</b>	Increase in thermal conductivity by a factor of 5 to 10; a reduction in the coefficient of thermal expansion by a factor of 2 to 3.
<b>Critical Materials</b>	Diamond-coated components; high thermal conductivity ceramics.
<b>Unique Test, Production, Inspection Equipment</b>	Chemical vapor deposition (CVD) equipment for the deposition of diamond films.
<b>Unique Software</b>	None identified.
<b>Technical Issues</b>	Use of materials with high thermal transfer (e.g., diamond-coated tube components).
<b>Major Commercial Applications</b>	Space electronics and radar systems.
<b>Affordability</b>	Not an issue.

#### ***RATIONALE***

All mmW components generate heat, and the dissipation of this heat is important for the proper operation of the components. Continued improvements in these devices will depend, along with other developments, on improved methods to dissipate heat. TMD Technologies Limited (United Kingdom), has announced preliminary results of research in which components of the microwave devices have been coated with diamond films. Initial results indicate that the CVD diamond offers increased electrical resistivity combined with a tenfold increase in thermal conductivity and a decrease in the coefficient of thermal expansion.

#### ***WORLDWIDE TECHNOLOGY ASSESSMENT***

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 United States      ●●

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Legend:      Extensive R&D      ●●●●      Significant R&D      ●●●      Moderate R&D      ●●      Limited R&D      ●

### DATA SHEET III-8.1. MILLIMETER-WAVE (mmW) TRAVELING WAVE TUBES (TWTs)

<b>Developing Critical Technology Parameter</b>	Frequency > 90 GHz; output power ≥ 200 W average; weight < 20 kg; bandwidth ≥10%.
<b>Critical Materials</b>	Scandate (Sc <sub>2</sub> O <sub>3</sub> ) cathodes; diamond-coated rods; Samarium Cobalt magnets; high thermal conductivity ceramics.
<b>Unique Test, Production, Inspection Equipment</b>	Machine (including micromachines) tools to manufacture the TWT components.
<b>Unique Software</b>	CAD/CAM.
<b>Technical Issues</b>	Improved cathodes; improved cooling (perhaps diamond); improved magnets for better focusing.
<b>Major Commercial Applications</b>	Space electronics; radar systems.
<b>Affordability</b>	Not an issue.

#### ***RATIONALE***

TWTs are essential components in radar, EW, countermeasures, missile electronics, UAVs, communications, and space applications. Research is being conducted to address the following characteristics: broad bandwidth, high efficiency, high gain, high voltage stand-off capability, low noise, compact size, low weight, lower cost, and improved reliability.

#### ***WORLDWIDE TECHNOLOGY ASSESSMENT***

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Russia	• • •	UK	•	United States	• • •		
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### DATA SHEET III-8.1. MICROWAVE POWER MODULES (MPMs)

<b>Developing Critical Technology Parameter</b>	Power greater than 1.5 kW in X-band; power greater than 1 kW in I/J-band; efficiencies greater than 50 percent; size/weight less than one-fifth of conventional TWTs.
<b>Critical Materials</b>	Silicon or gallium arsenide for the integrated circuits (ICs).
<b>Unique Test, Production, Inspection Equipment</b>	Standard equipment for the manufacture of ICs; machine tools for the manufacture of the TWT components.
<b>Unique Software</b>	CAD/CAM.
<b>Technical Issues</b>	High gain of MMICs; lower cathode voltage of helix TWTs; power conditioning systems.
<b>Major Commercial Applications</b>	Space electronics and radar systems.
<b>Affordability</b>	Not an issue.

#### ***RATIONALE***

The MPM is capable of providing high power over wide bandwidths at high efficiency. It is also smaller and less expensive than conventional TWTs. Initial and projected military applications include X-band radar, EW, UAVs, and communication systems.

MPMs include three basic parts: a vacuum power booster (VPB) (a helix TWT), a solid-state amplifier (SSA) (an MMIC), and an EPC. The EPC converts the input voltage to the proper operating voltages for the VPB and the SSA and monitors the condition of the module. The SSA receives the RF input, amplifies it, and provides the RF drive to the VPB. The VPB provides the high-power RF output.

#### ***WORLDWIDE TECHNOLOGY ASSESSMENT***

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Japan	••	Netherlands	•	UK	•	United States	••••
<hr/> Legend:      Extensive R&D    ••••    Significant R&D    •••    Moderate R&D    ••    Limited R&D    •							

## SECTION 8.2—ELECTRONIC MATERIALS

### *Highlights*

- Separation by the Implantation of Oxygen (SIMOX) silicon-on-insulator (SOI), made by high-energy implantation of oxygen into a heated silicon substrate, results in a thin layer of silicon separated from the substrate by an insulating layer of silicon dioxide.
- SiC-based electronics and sensors can operate in hostile environments where conventional silicon-based electronics (limited to 350 °C) cannot function.

### **OVERVIEW**

This technology area includes preparing and processing new and current electronic materials from the purification of the basic elements to the final wafer or substrate material ready for device fabrication. Materials handling and their processes are currently undergoing rapid changes to meet the future demands of the electronic industry. These materials are made of very pure starting materials.

Depending on the material under consideration, preparation methods are numerous, including SIMOX made by high-energy implantation of oxygen into a heated silicon substrate. SIMOX wafers are created by implanting oxygen atoms below the surface of a silicon wafer in sufficient quantity to transform the silicon-to-silicon dioxide. After implantation, the wafers are carefully annealed at high temperatures, typically 1,325 °C, to repair defects introduced by the oxygen implantation and to crystallize the silicon dioxide. The insulating silicon dioxide separates the top silicon layer from the substrate, and ICs are then fabricated in the top silicon layer. A second method used to form SOI uses ion implantation and wafer bonding technologies. Starting with two wafers, the silicon surface of one wafer is first oxidized to form what will become the buried oxide layer of the SOI structure. An ion implantation step, using hydrogen ions, is then executed through the oxide layer by a standard high-current ion implanter to form a usable thin layer of silicon and a layer of microbubbles at the path length of the hydrogen implant. The second wafer is then bonded to the oxide layer. The sandwiched wafers are thermally treated and break apart at the micro-bubble layer, which is then annealed and polished. The surface silicon of the finished wafer has very low defect levels that approach those in bulk silicon. The oxide layer is pinhole free.

The successful growth of heteroepitaxial SiC with high resistivities and low-defect densities, improved epilayer doping, and thickness control on large area substrate materials [greater than 3 in. using metallo organic chemical vapor deposition (MOCVD)] and epitaxial growth equipment are critical to military electronics.

### **RATIONALE**

An important military application of SOI technology is its increased radiation hardness, particularly in the area of dose rate survivability and single-event upset (SEU). Additional advantages of this technology include performance (speed) improvements, size reductions, and increased temperature range. COTS chip sets are not sufficiently radiation resistant, use too much power, or do not have required reliability for long-duration space missions. The insulating layer isolates the active transistors from the silicon substrate and gives the chip set very high immunity from high-radiation dose rates created by nuclear detonations, which could cause transient or permanent failure in the processor. Further development of circuits optimized for SOI could yield much greater performance results, while reducing chip size and power consumption.

IBM has forecasted that SOI would offer a 20-percent performance improvement because of reduced capacitance (a by-product of having a thin oxide layer under the transistors) and is working the development of a gigahertz-level microprocessor. In addition, metal-oxide semiconductor field-effect transistors (MOSFETs) made in thin-film SOI substrates present very small junction areas, and their high-temperature leakage current can be 3 to 4 orders of magnitude lower than those of regular metal-oxide semiconductor (MOS) devices. The functionality of 16-K and 256-K static random access memories (SRAMs) at high temperatures (up to 300 °C) and of SOI comple-

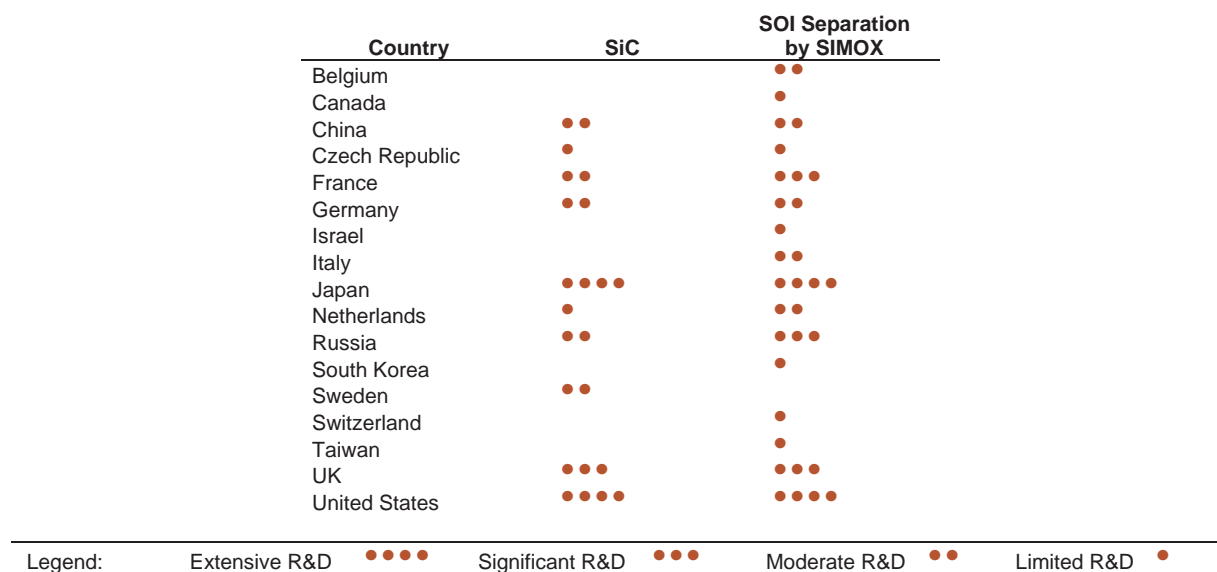
mentary metal-oxide semiconductor (CMOS) ring oscillators up to 500 °C has been demonstrated. The ability of SiC to function in high-temperature, high-power, and high-radiation environments will enable large performance improvements to a wide variety of military systems and applications.

IBM, one of the leaders in the development of this technology, believes the low-power aspects of SOI technology will be key to the creation of multifunction, handheld “information appliances” of the future. Although the technology behind SOI has been explored for some time, technical hurdles made its application in high-volume, mainstream chip making difficult and expensive. IBM claims that its approach allows SOI to be used in mainstream semiconductor manufacturing, with few changes or additions to existing fabrication lines and at little additional cost.

The new process represents the culmination of more than 15 years of collaboration between IBM research and the company’s manufacturing and development teams. Two major changes were made to effect this development. On the substrate itself, the implant and anneal steps were optimized to get the lowest defect per density. In addition, the device design and the process were optimized to fabricate “partially depleted” SOI devices, where the undesirable effects (e.g., the floating body effect) can be addressed.

In terms of development work, Motorola, Inc., is said to be using the material at some level for wireless communication chips in pilot-scale operations. The company is already home to at least one Ibis Technology Corporation implanter. They could be moving SOI into production sometime in the near future. Honeywell has also placed some emphasis on SOI. The company, which has close ties to SOI wafer supplier Silicon-On-Insulator Technologies (SOITEC) of France, has been putting more and more of its CMOS devices into SOI.

**WORLDWIDE TECHNOLOGY ASSESSMENT (see Figure 8.2-1)**



**Figure 8.2-1. Electronic Materials WTA Summary**



**LIST OF TECHNOLOGY DATA SHEETS**  
**III-8.2. ELECTRONIC MATERIALS**

Silicon Carbide (SiC) .....	III-8-19
Silicon-on-Insulator (SOI) Separation by the Implantation of Oxygen (SIMOX) .....	III-8-21



### DATA SHEET III-8.2. SILICON CARBIDE (SiC)

<b>Developing Critical Technology Parameter</b>	SiC-based electronics and sensors can operate in hostile environments where conventional silicon-based electronics (limited to 350 °C) cannot function. The performance of these devices is severely degraded at elevated temperatures, at the highest RF powers, and in harsh radiation conditions. SiC's ability to function in high-temperature, high-power, high-frequency, and high radiation conditions will enable large performance improvements to a wide variety of military systems and applications. These include solar blind detectors; microwave/millimeter radar; communication; EW and missile seeker systems; high-current, high-voltage; and high-speed requirements of CW and pulsed electrical subsystems in emerging hybrid-electric and all-electric combat vehicles, more electric airplanes, and naval ships. Research is focused on developing the base crystal growth and device fabrication technologies necessary to produce a family of SiC high-temperature, high-power electronic devices and circuits to meet system demands for hostile environment.
<b>Critical Materials</b>	SiC bulk crystals; thin films of epitaxial-grown SiC.
<b>Unique Test, Production, Inspection Equipment</b>	MOCVD; epitaxial growth equipment; bulk and surface lifetimes measuring systems for ultrathin films; spectroscopic ellipsometer; spectrophotometer; defect detection and classification equipment; interferometric measurement equipment.
<b>Unique Software</b>	Special algorithms to control the growth process of the materials; metrology equipment software.
<b>Technical Issues</b>	Increase substrate diameter (6 in.) with high ( $10^8$ ) resistivity for microwave applications; control resistivity of epilayer; reduce dislocation and micropipe densities. Higher growth rates ( $> 5 \mu\text{m/hr}$ ) while maintaining high quality, accurate and reproducible process control, homogeneity of all relevant properties, electrical characteristics and yields, are necessary for SiC devices to be considered more than just a niche market.
<b>Major Commercial Applications</b>	Capability of operation in the 600-°C region at power levels of 1,000 V and current densities exceeding $1,000 \text{ A/cm}^2$ provides electronic devices and circuits to meet system demands for hostile-environment electronics. In addition, solid-state electronics have to improve the transmission, distribution, and quality of electric power in the utilities Industry.
<b>Affordability</b>	In addition to substrate price, the development of an inexpensive epitaxial process for SiC is a major precondition for manufacturing SiC devices at a lower cost.

#### ***RATIONALE***

Conventional semiconductor electron devices, such as field-effect transistors (FETs), are fabricated using silicon or compound semiconductors, such as GaAs. The performance of these devices is severely degraded at elevated temperatures and in harsh environments where harmful radiation may be present.

In the last decade, a concerted worldwide effort has emerged to develop the next generation of electronic devices that would be able to operate at elevated temperatures and in harsh environments (e.g., outer space). Such devices would be fabricated using semiconductor materials that have a large bandgap [more than 2 eV (i.e., about twice that of conventional semiconductors such as silicon and GaAs)]. Examples include SiC and diamond. Unlike silicon, SiC-based devices can operate reliably in environments in excess of 150 °C and are capable of operation in the 600-°C region. The use of SiC eliminates the need for remote cabling or cooling systems by enabling devices to function in the hot areas of high-speed airframes, aircraft, and internal combustion engines and in other macro devices, platforms, and systems that operate at temperatures in excess of 400 °C. In the field of power electronics, SiC distinguishes itself as being capable of handling several thousand volts in reverse mode and at least  $1,000 \text{ A/cm}^2$  in forward mode for use in high-power switches operating at 1,000 V and at current densities exceeding

1,000 Å/cm<sup>2</sup>. Specific issues that need to be resolved include suitable “substrate” for epitaxial growth, suitable dopants for p- and n-type materials, reduction of dislocations that arise in epitaxial layers because of differences in the lattice constants and in coefficients of thermal conductivity, and the ability to grow materials over large wafer areas. This technology is accessible through U.S. government agencies and commercial companies.

#### ***WORLDWIDE TECHNOLOGY ASSESSMENT***

China	• •	Czech Republic	•	France	• •	Germany	• •
Japan	• • • •	Netherlands	•	Russia	• •	Sweden	• •
UK	• • •	United States	• • • •				

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Legend:      Extensive R&D    • • • •      Significant R&D    • • •      Moderate R&D    • •      Limited R&D    •

## DATA SHEET III-8.2. SILICON-ON-INSULATOR (SOI) SEPARATION BY THE IMPLANTATION OF OXYGEN (SIMOX)

<b>Developing Critical Technology Parameter</b>	More precise, high-energy oxygen implantation technology for the production of 200- to 300-mm-diameter wafers with thin single crystal silicon (less than 1000 Å) and oxide insulating layer (less than 300 Å by the year 2006) wafers (see <b>Background</b> ).
<b>Critical Materials</b>	Large area (200- to 300-mm) silicon wafers.
<b>Unique Test, Production, Inspection Equipment</b>	High-energy (250 keV) oxygen and low-energy (100 keV) hydrogen implanters; atomic absorption; X-ray reflective measuring equipment.
<b>Unique Software</b>	Ion implantation beam; metrology; diagnostic software.
<b>Technical Issues</b>	High-energy implantation of oxygen into a heated substrate of silicon (known as SIMOX). Wafers are created by implanting oxygen atoms below the surface of a silicon wafer in sufficient quantity to transform the silicon to silicon dioxide (SiO <sub>2</sub> ). SOI wafers are also fabricated using a chemical bonding UNIBOND® technique, which involves two wafers in combination with a hydrogen implant (see <b>Background</b> ).
<b>Major Commercial Applications</b>	Low-power, high-speed, and high-temperature applications (see <b>Background</b> ).
<b>Affordability</b>	Cost of SOI wafers is basically twice the cost of bulk silicon. The primary benefit commercializing SOI will be the reduced starting material costs and the producibility of SOI starting material.

### **RATIONALE**

SiO<sub>2</sub> films play a central role in semiconductor technology. SiO<sub>2</sub> is used as a very thin film separating the gate electrode and the Si substrate in complementary metal-oxide semiconductor field-effect transistors (CMOS FETs). The CMOS FET is an essential device for most ICs, including gate arrays, microprocessors, dynamic random access memory (DRAM), flash memories, silicon-on-chip system ICs, and so forth. The SiO<sub>2</sub> film's resistance against degradation is crucial to the reliability of the CMOS-FETs and, hence, to the IC chips themselves. The thickness of the film is an important parameter in determining the performance (signal speed) and level of integration. To reach the level of 4 Gbits/chip DRAM integration and performance level, the SiO<sub>2</sub> thickness must be scaled down from its present thickness of 3.5 nm to a thickness of approximately 2 nm.

Advantages of SOI technology include high speed, size reduction, and increased temperature range. An important military space application of SOI technology is its increased radiation hardness, particularly in the areas of dose rate survivability, and SEU. Advanced gigahertz-level microprocessors are capable of surviving high radiation dose rates. The SIA NTRS estimates that IC manufacturers will continue to use SiO<sub>2</sub> as gate-dielectric material up to the 4 Gbits/chip DRAM level. New materials are expected to replace SiO<sub>2</sub> above that level. Technology is available from U.S. companies, such as IBM and Motorola, Inc.

### **WORLDWIDE TECHNOLOGY ASSESSMENT**

Belgium	••	Canada	•	China	••	Czech Republic	•
France	•••	Germany	••	Israel	•	Italy	••
Japan	••••	Netherlands	••	Russia	•••	South Korea	•
Switzerland	•	Taiwan	•	UK	•••	United States	••••

Legend:	Extensive R&D	••••	Significant R&D	•••	Moderate R&D	••	Limited R&D	•
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## **BACKGROUND**

High-energy implantation of oxygen into a heated substrate of silicon is known as SIMOX. Standard SIMOX wafers are created by implanting oxygen atoms below the surface of a silicon wafer in sufficient quantity to transform the silicon to  $\text{SiO}_2$ , while maintaining a thin surface layer of circuit-quality, single-crystal silicon. After implantation, the wafers are carefully annealed to repair defects introduced by the oxygen implantation and to crystallize the  $\text{SiO}_2$ . The insulating  $\text{SiO}_2$  separates the top silicon layer from the substrate, and ICs are then built in the top silicon layer.

One important military space application of SOI is its increased radiation hardness, particularly in the area of dose rate survivability and SEU. Additional advantages of SOI technology include performance (speed) improvements, size reductions, and increased temperature range. COTS chip sets are not sufficiently radiation resistant, use too much power, or do not have required reliability for long-duration space missions. The insulating layer that isolates the active transistors from the silicon substrate gives the chip set very high immunity from high-radiation dose rates created by nuclear detonations, which could cause transient or permanent failure in the processor. Further development of circuits optimized for SOI could yield much greater performance results, while reducing chip size and power consumption. Because of the hardness of SOI to all radiation environments, this technology spans the full range of high-reliability space applications.

High-temperature space applications are also a concern. Thermal shielding for satellites is quite heavy, and the weight of a satellite has a direct impact on the cost of placing it in orbit. In some special applications (Venus probes), shielding is no longer possible, and high-temperature electronics are absolutely required. Much higher temperature tolerance is required from engine-monitoring electronics, such as electronic injection systems, where precision control of the injector position is controlled by electronic components located close to or within the engine block. Modern antilock braking systems (ABSs) also require electronic control systems placed close to the brakes, and these systems are exposed to high temperatures when the brakes are activated. The ability of SOI CMOS to operate at high temperatures, combined with the possibility of integrating power devices with low-power logic on a single, dielectrically isolated substrate, renders SIMOX the ideal technology for such purposes. High-temperature airplane applications include onboard electronics and, of course, engine control and surface control (wing temperature).

The production of UNIBOND® wafers uses both ion implantation and wafer bonding technologies. Starting with two wafers, the silicon surface of one wafer is first oxidized to form what will become the buried oxide layer of the SOI structure. An ion implantation step using hydrogen ions is then executed through the oxide layer by a standard high-current ion implanter to form a usable thin layer of silicon and a layer of microbubbles at the path length of the hydrogen implant. The second wafer is then bonded to the oxide layer. The sandwiched wafers are thermally treated and break apart at the microbubble layer, which is then annealed and polished. The surface silicon of the finished wafer has very low defect levels that approach those in bulk silicon. The oxide layer is pinhole free. The remaining wafer, which is still within Semiconductor Equipment and Materials International (SEMI) standards for thickness specifications, is reclaimed and polished. It is then used as the support wafer for producing the next UNIBOND® wafer.

This SOI UNIBOND® technology solves the two limitations of conventional bonding. The uniformity for thin SOI layers is obtained because ion implantation is used, and, since the second wafer is saved, the traditional wafer-bonding cost barrier caused by the consumption of two starting wafers to produce one SOI wafer is eliminated.

## SECTION 8.3—ELECTRONICS FABRICATION

### *Highlights*

- Lithographic technologies use 193-nm ultraviolet (UV) lithography and EUV lithography (EUVL) for fabrication devices with line widths of 100 nm.
- Lithographic technologies use proximity X-ray, electron beam (e-beam) projection, electron-beam direct write (EBDW), and ion projection for the fabrication of semiconductor devices.
- Lithographic technologies can generate and transfer highly complex patterns for MEMS.
- Nanotechnology provides the capability to design, fabricate, and test electronic devices with critical feature sizes below 0.1  $\mu\text{m}$ .
- MEMS technology enables the development of chemical, biological, and mechanical smart systems.
- Specially designed semiconductor processing modules provide a unique integrated system for sequential multiple processing of wafers in a vacuum environment.

### **OVERVIEW**

This section addresses the developing semiconductor processing equipment technologies used to fabricate devices for military systems. (The same process is used in commercial fabrication.) The technologies will either provide a superior final device or reduce the cost of fabricating the existing device. These technologies involve the growth of epitaxial layers, implantation of dopants, the use of cluster tools for the deposition and etching of thin-film layers, single-wafer processing, delineation of patterns using lithographic techniques, and testing and packaging of ICs. They are also used for passive and active devices, MEMS, and sensors in military equipment and systems.

Optical lithography continues to be the mainstream technology for the semiconductor industry and is being used in production at 250-nm design rules. Extensions of optical technology are being used to support 180-nm product and process development. Advanced technologies, such as X-ray and EBDW, have been used to fabricate functional semiconductor devices below 100 nm over small field sizes at low throughput. In addition, various technologies have been proposed, and studies are underway for resolution capability down to 50 nm.

One promising technology that builds on the optical experience is EUVL using 10- to 14-nm soft X-ray photons; however, overlay and critical dimension (CD) improvements have not kept pace with resolution improvements. The estimates for overlay appear to plateau around 30 nm. This will be inadequate for ground rules less than 100 nm. Overlay and CD control over large field sizes will continue to be a major concern for < 130-nm lithography. Continuous improvements in mask-making technology (mask writers, inspection, repair, and substrates) continue to be required to support the technical and manufacturing needs of optical lithography below 250 nm.

MEMS include sensors and actuators that are fabricated using IC production processes. Automotive, biomedical, aerospace, and robotic MEMS devices are produced with combinations of bulk and surface micromachining. MEMS processing uses these technologies to create structural components that are essentially submillimeter-sized machine parts. High-energy oxygen implanters are used to produce SOI wafers—a technology that has long been relegated to radiation-hardened circuits for military and space environments, a small niche market. Ion implanters to be used in fabricating large-area SOI wafers for the development of gigahertz-level microprocessors are being developed. SOI would offer a 20- to 35-percent performance improvement because of reduced capacitance, a by-product of having a thin oxide layer under the transistors.

### **RATIONALE**

Semiconductor technology is one of the key areas that gives the United States superior military capabilities. It is one of the most crucial and pervasive technologies contributing to the current technological edge that U.S.

systems have over systems of adversary countries. These technologies are used in the production of every weapon system in the U.S. arsenal and enable dramatically higher performance and reliability with smaller size and less weight.

Lithography involving wafer delineation, resist processing, and mask making is the prime determinant of feature size and, hence, density of ICs and is therefore one of the most critical elements in the high speed and high density required for today's military systems. Cluster tools can be used for plasma-enhanced CVD, dry etch, high-pressure oxidation, rapid thermal anneal, and numerous other processes either as a batch system performing one process or as a system doing sequential processing steps. Processes that could not be done by using standalone systems can now be done using a cluster tool. Microcircuits, sensors, and active and passive semiconductor devices are widely used in military systems for this reason and are common in missiles, avionics, torpedoes, smart munitions, proximity fuses, sonobuoys, and secure communication satellites.

### ***TECHNOLOGY ASSESSMENT***

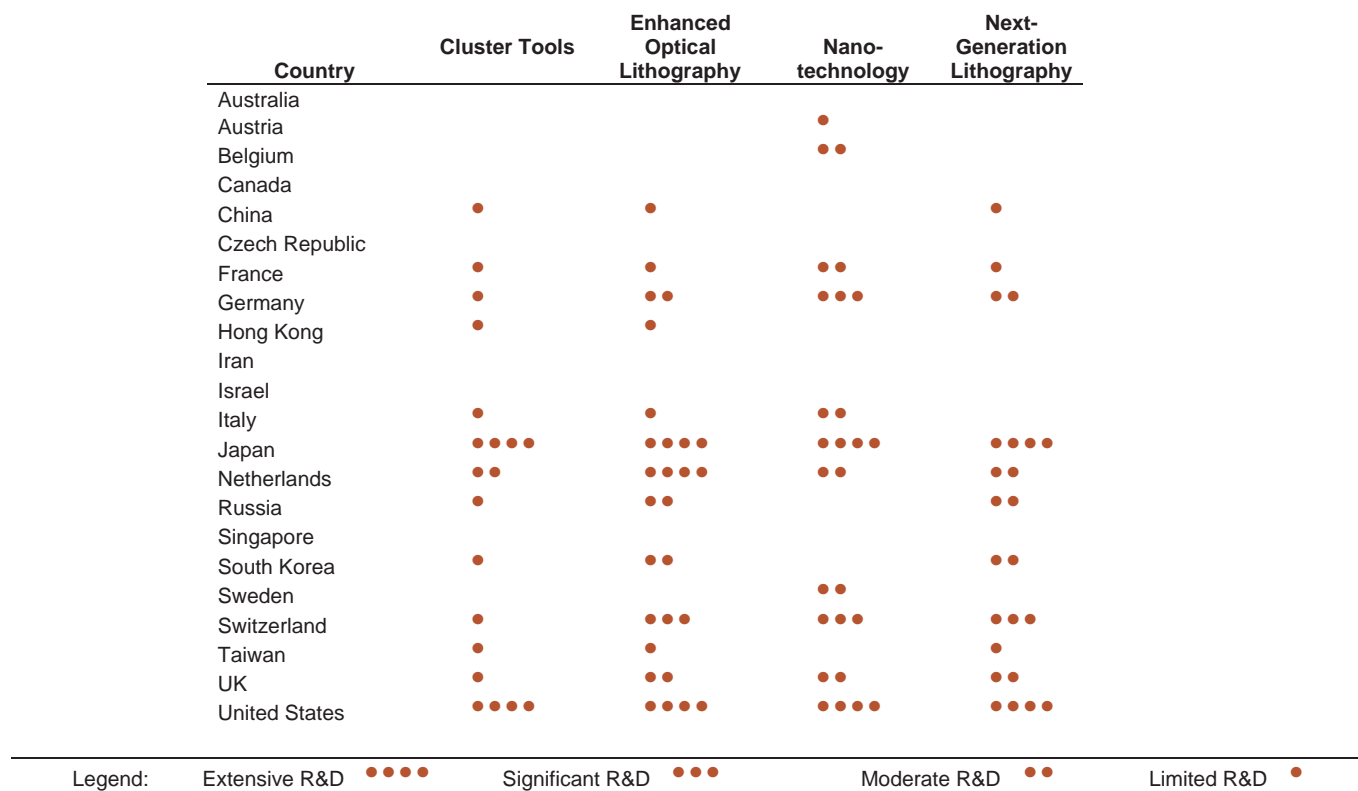
Deep ultraviolet (DUV) 248-nm lithography has recently demonstrated the ability to print features as small as 100 nm (0.10  $\mu\text{m}$ ). Argon-fluoride (ArF) excimer laser 193-nm lithography, still in the development stage, requires new lens designs, new lens materials, and new resist chemistries. Critics claim that it is far too expensive for economical production. Supporters of 193-nm lithography point out that extending DUV is also expensive. At 100 nm, DUV exposure requires optical proximity correction (OPC) and phase-shifting masks (PSMs). OPC adds subresolution features to the mask to correct for printing and etching errors, increasing the mask write time. Both techniques increase the mask cost. The cost of a complete DUV mask set for the 130-nm technology node could exceed \$500,000. While such costs are tolerable for high-volume products (e.g., memories), they are prohibitive for many other applications. Although 193-nm lithography still requires resolution enhancements, such as OPC, the shorter wavelength offers improved depth of focus and widening of the process window.

It is expected that 193-nm lithography will be used for critical layers beginning with the 130-nm technology node, which is expected in production in 2001. This schedule coincides with current expectations for 300-mm production. However, few chipmakers are likely to introduce a new lithography technique and a new wafer size at the same time in the same lab. Current lithography uses a variety of techniques to make a mask that is used to etch the patterns on silicon to create the IC. Efforts are continuing to decrease the feature sizes and position errors on these masks.

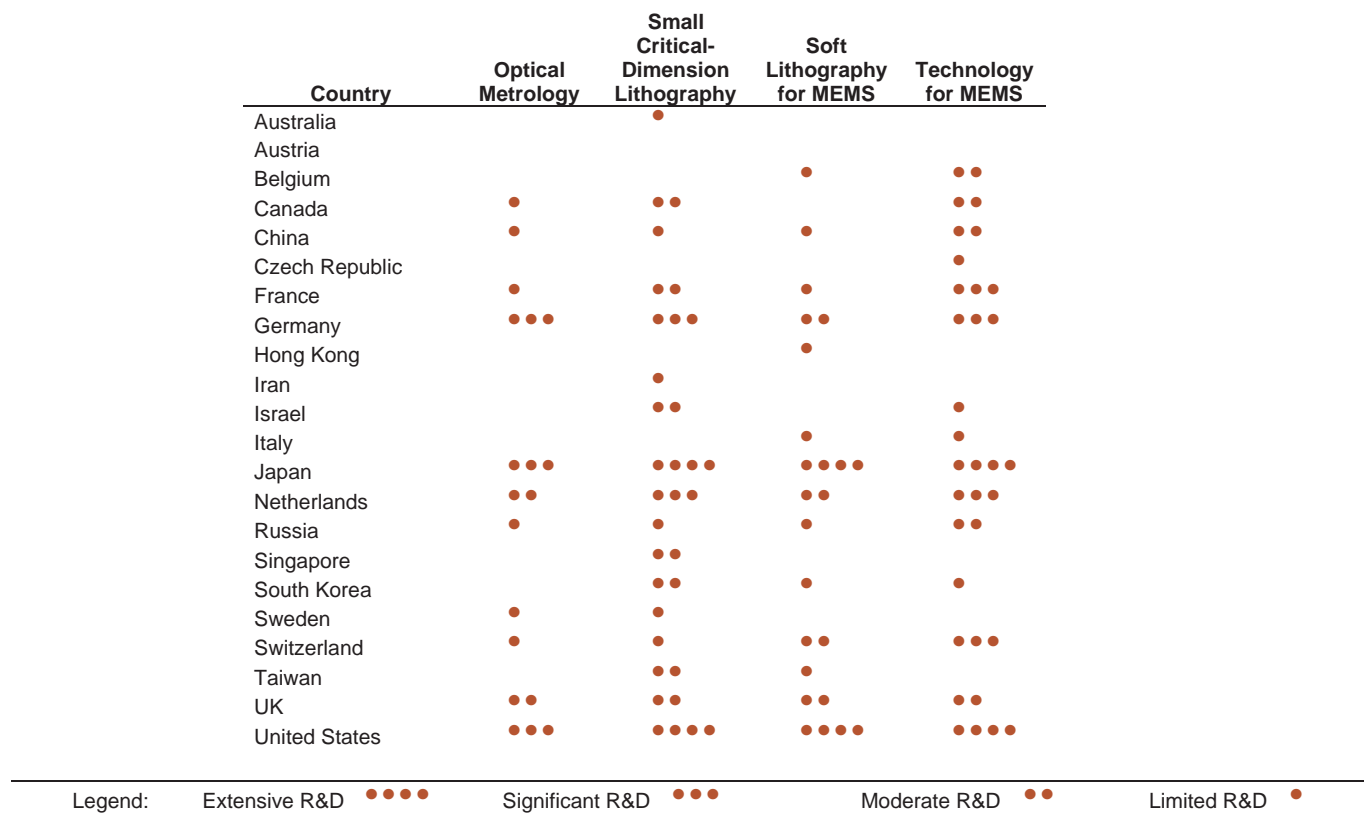
A fundamental breakthrough would be to enable maskless lithography. R&D programs are pursuing several approaches leading to direct computer control of parallel electron beams for maskless patterning of wafers. Another approach has been the use of supersonic gas jets for direct patterned deposition of semiconductor material, thus eliminating several resist and etch processing steps. These maskless lithography developments offer faster prototyping and reduced fixed costs for the low-volume production typical of military systems.



**WORLDWIDE TECHNOLOGY ASSESSMENT** (see Figure 8.3-1)



**Figure 8.3-1. Electronics Fabrication WTA Summary (1 of 2)**



**Figure 8.3-1. Electronics Fabrication WTA Summary (2 of 2)**

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### DATA SHEET III-8.3. CLUSTER TOOLS

<b>Developing Critical Technology Parameter</b>	Cluster tools will enable an extensive set of sub-0.15µm gate, capacitor, and shallow trench isolation applications, with excellent CD control, operational flexibility, and damage-free results for sub-0.15µm device designs with sub-20Å gate oxides. Cluster tools' superior degree of process control offers high-etch-rate in situ process integration capability, near vertical profiles, high selectivity of substrates, and excellent repeatability of results. The tools' new controllable magnetic field technology and advanced temperature control will provide uniform, damage-free results over an extremely broad operating window. The systems' advanced and emerging interconnect technology (in situ damascene integration, main dielectric etch/PR and polymer removal/nitride barrier removal, copper interconnects, low-k dielectrics, and advanced contacts) provides chip makers with next-generation 0.10-µm extendibility that delivers high throughput, enhanced reliability, and the flexibility to deliver advanced applications for new and emerging interconnect technologies. In addition, upgrades and retrofits are available for existing tools to facilitate the deposition and etch solutions needed for 0.15 µm, 0.10 µm, and beyond.
<b>Critical Materials</b>	Surface finish of metal components, hardness, and chemical inertness; outgassing properties; dimensional stability.
<b>Unique Test, Production, Inspection Equipment</b>	Real-time closed loop in situ automated process control; defect detection and classification; wafer tracking and transport; communication standardization.
<b>Unique Software</b>	Specially designed algorithms for process control.
<b>Technical Issues</b>	Maintaining environmental integrity between process modules; surface finish of metal components, hardness, and chemical inertness; outgassing properties; dimensional stability.
<b>Major Commercial Applications</b>	For the semiconductor industry, integrated processing was the newest technology driver of the 1990s, and cluster tools became the vehicles for implementing the concept. In the next few years, more and more IC processes will be implemented in cluster systems—not only for the most often-cited reasons (contamination control, yield improvement, throughput, and so forth) but also because of increasing competitive pressure on the world's semiconductor manufacturers for improved, economically efficient manufacturing.
<b>Affordability</b>	The cost of cluster tools is very high. They remain a major precondition for manufacturing state-of-the-art ICs.

#### **RATIONALE**

Cluster tools are semiconductor fabrication processing systems that have some of the following unique features: a stored program, controlled, automatic loading central wafer handling system; specially designed interfaces for wafer input and output; specially designed semiconductor processing modules or chambers capable of doing process steps such as epitaxial growth, CVD, physical vapor deposition (PVD), etch, oxide growth, passivation, and anneal; a communication system that provides an integrated system for sequential multiple processing of wafers in a vacuum environment; single wafer and sequential multiwafer processing; and sequential batch processing. Cluster tools can be divided into two areas:

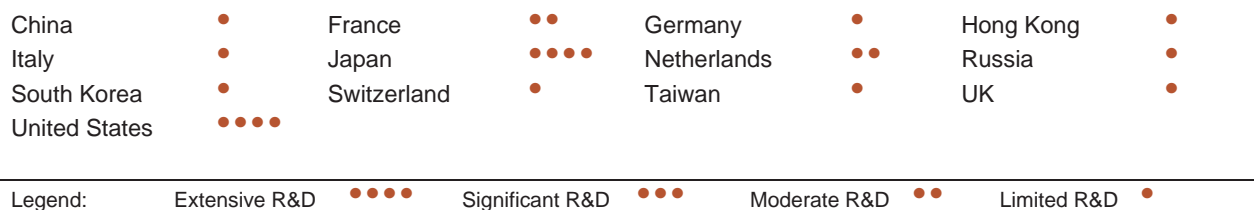
- A highly sophisticated system that provides an integrated system for sequential multiple processing of wafers
- A system that does batch processing where one processing step (i.e., deposition or etch) takes place in a highly controlled environment.

The evolution of cluster tools has progressed from the addition of load locks and process systems, to load lock, preclean, process, and passivation, to the integration of more than one process step in the same system. Cluster tools can be used for plasma-enhanced CVD, dry etch, high-pressure oxidation, rapid thermal anneal, and numerous other processes either as a batch system performing one process or as a system performing sequential processing steps. Processes that could not be done using standalone systems can now be done using a cluster tool (e.g., the selective deposition of tungsten).

With an integrated process, one can first use an etch chemistry to remove any ambient-formed oxide and condition the silicon surface at the bottom of the plug (because tungsten does not adhere well to silicon oxide) and then immediately begin growing tungsten. Both steps can take place under vacuum and in rapid sequence, thus inhibiting the formation of oxide layers between films, which reduce selectivity and increase contact resistance. Military devices for microwave, mmW, and high-speed digital FETs for real-time signal processing devices for EW systems would be seriously degraded without this processing step. Microwave diodes, such as IMPATT (IMPact Avalanche Transit-Time), Gunn, TRAPATT, (TRApped Plasma Avalanche Transit-Time), PIN (Positive-Intrinsic-Negative), and CATT (Controlled Avalanche Transit-Time), primarily used in phased-array radar, personnel detection, weapons delivery, digital communication, and miniature jammers, could not be fabricated reliably or with the same properties without cluster tools.

DoD has always recognized the criticality of cluster tools in providing the military with low-volume, leading-edge devices; however, DoD is not the only market for low-volume devices. In the near future, lithography clusters capable of robotically changing and aligning a reticle in less than 1 min will be in commercial production lines and will enable manufacturers to have wafers with different devices in the same batch. Because the days of commercial production lines dedicated to military circuits are coming to an end and military systems are using more COTS parts, the capability for low-volume production becomes very important. This capability serves the low-volume requirements of the military and the commercial sectors. With the transition to larger 300-mm wafer sizes, single wafer processing tools have become a requirement to maintain reliable process control. In these systems, multiple process modules, each independently processing individual wafers, cluster around a single wafer handler.

## WORLDWIDE TECHNOLOGY ASSESSMENT



## BACKGROUND

In the mid-1980s, the military was faced with the problem of obtaining spare part semiconductor devices for equipment that had been developed and fielded 20 years ago. The processing lines that produced these devices no longer existed, and the inventory of spare parts was quickly dwindling. The military realized that the devices developed and produced during the Very High-Speed Integrated Circuit (VHSIC) program would face the same fate because it was not economically feasible for semiconductor manufacturers to maintain militarily certified production lines to produce a relatively small quantity of devices.

The individual Services took different approaches to the problem of replacing spare parts—a problem that exists to this day. At the Naval Ocean Systems Center (NOSC) in San Diego, California, the Navy built small pilot lines to duplicate past processes and fabricate the required spare parts. The Army at Fort Monmouth, New Jersey, in cooperation with LSI Logic, duplicated the function of the required spare parts by using LSI Logic's design software and their ASIC devices. The Air Force immediately started stockpiling finished wafers of devices used in their systems. However, they soon realized that this would not be a viable solution and, in 1988, awarded a \$112 million contract for a Microelectronics Manufacturing Science and Technology (MMST) program to Texas Instruments to develop new, creative, and cost-effective solutions for manufacturing low-volume military ICs, microwave devices, and sensors. The program's goals of rapid cycle time, low-volume capability, and process flexibility required replacing traditional batch processing equipment with single wafer processing equipment.

### DATA SHEET III-8.3. ENHANCED OPTICAL LITHOGRAPHY

<b>Developing Critical Technology Parameter</b>	Lithographic technologies for the generation and transfer of highly complex patterns for microelectronics and micromechanical structures using 157-nm UV lithography and EUVL employing 10–14 nm soft X-ray photons [see <b>Background; Lithographic Requirements (Table 8.3-1); Extreme Ultraviolet Lithography (EUVL)</b> ].
<b>Critical Materials</b>	Advanced resist systems (bi-layer, thin-layer imaging, chemically amplified); optical materials; antireflective materials for optical; EUVL.
<b>Unique Test, Production, Inspection Equipment</b>	Optical, EUVL exposure equipment; phase shift masks; mask inspection equipment; wafer level defect recognition and analysis.
<b>Unique Software</b>	Defect recognition and analysis; OPC; statistical quality control (SQC).
<b>Technical Issues</b>	Alignment and registration accuracy; minimum resolvable feature size; increased depth of focus; exposure source integrity; process-generated defects; mask inspection; mask defect repair; metrology equipment for critical dimension and overlay. Military requirements not being addressed by the commercial sector are focal plane arrays (FPAs) with unique infrared (IR) requirements for military electronics and sensors.
<b>Major Commercial Applications</b>	Lithography is used in fabricating all semiconductor devices, ICs, and MEMS devices.
<b>Affordability</b>	Not an issue.

#### RATIONALE

Lithography is the enabling technology that has supported the IC industry for decades. Lithography and micropattern transfer technology used to fabricate devices and ICs are the keys in determining their performance and maintaining a strategic edge in a wide range of military sensors, EW devices, communications, command and control (C2), and offensive and defense weapon systems. New, advanced lithographic technologies are required to adhere to the advanced performance projections for IC devices in the 21<sup>st</sup> century.

#### WORLDWIDE TECHNOLOGY ASSESSMENT

China	•	France	•	Germany	••	Hong Kong	•
Italy	•	Japan	••••	Netherlands	••••	Russia	••
South Korea	••	Switzerland	•••	Taiwan	•	UK	••
United States	••••						

Legend: Extensive R&D •••• Significant R&D ••• Moderate R&D •• Limited R&D •

#### BACKGROUND

#### LITHOGRAPHIC REQUIREMENTS

Optical lithography (nominally defined for wavelengths of 157 nm and greater) continues to be the mainstream technology for the semiconductor industry. It is about to enter in production at 180-nm CD design rules. Improvements to optical technology will be required to support product and process development at CDs of 180 nm and below. Resolution enhancement techniques (RETs) include wavelength reduction (193 nm–157 nm) and off-axis illumination, as well as PSM and OPC. The key challenge to optical enhancement at the 130-nm CD level will be maintaining an adequate and affordable process latitude (depth of focus/exposure window) necessary for 10-percent post-etch CD control. Mask-making capability exists for 250-nm generation chrome binary masks. Capability for

complex PSM, OPC, and 180-nm binary masks are in development and pilot production. Solutions for rapidly growing data volumes need to be developed, especially for optical proximity correction in the < 250-nm regime. Advanced I-line resists are in manufacturing, with resolution capabilities down to 300 nm. DUV resists at 248 nm are commercially available and are being used to manufacture 64-MB DRAM and MPU products.

Overlay requirements are among the most difficult technical challenges in lithography. Overlay and CD improvements have not kept pace with resolution improvements. The estimates for overlay appear to plateau around 30 nm, which will be inadequate for ground rules less than 100 nm. Overlay CD control over large field sizes continues to be a major concern for < 130 nm lithography. Advances in stage technologies, environmental controls, interferometers, and alignment systems will be needed for < 65 nm overlay. Continuous improvements in mask-making technology (mask writers, inspection, repair, and substrates) are required to support the technical and manufacturing needs of optical lithography below 250 nm. Table 8.3-1 lists projected advances in lithography and overlay.

Mask inspection requirements will become more aggressive as optical lithography pushes to finer resolutions. Major process and materials development is required to achieve the tolerances and mechanical properties necessary in the unique substrates used in these advanced technologies. Key issues will be identifying and repairing defects and the ability to keep masks defect free in manufacturing.

**Table 8.3-1. Critical Level Lithography Requirements**  
(Source: SIA NTRS)

Year of Production	1999	2001	2003	2006	2009	2012
Technology Generation	180 nm	150 nm	130 nm	100 nm	70 nm	50 nm
<i>Product Application</i>						
DRAM (bits)	1G	2G	4G	16G	64G	256G
MPU (logic transistors/cm <sup>2</sup> )	6M	10M	18M	39M	84M	180M
ASIC (usable transistors/cm <sup>2</sup> )	14M	16M	24M	40M	64M	100M
<i>Minimum Feature Size</i>						
MPU Gates (Isolated lines)	140	120	100	70	50	35
DRAM (Dense lines)	180	150	130	100	70	50
Contacts	200	170	140	110	80	60
Gates (nm, 3 sigma)	14	12	10	7	5	4
Overlay (nm, mean + 3 sigma)	65	55	45	35	25	20
<i>DRAM Chip Size (mm<sup>2</sup>)</i>						
Year 1	400	480	560	790	1120	1580
Year 2	320	390	450	630	900	1300
Year 3	240	290	340	480	670	950
<i>MPU Chip Size (mm<sup>2</sup>)</i>						
Year 1	360	400	430	520	620	750
Year 2	290	240	260	310	370	450
Year 3	220	240	260	310	370	450

### **EXTREME ULTRAVIOLET LITHOGRAPHY (EUVL)**

Optical lithography has provided the enabling technology to support the IC industry for several decades. However, new approaches will be required to maintain the Moore's Law projections for IC manufacturing in the 21<sup>st</sup> century. One promising technology, which builds on the optical experience, is EUVL using 10- to 14-nm soft X-ray photons. For these wavelengths and 4× reduction, low numerical aperture (NA) imaging systems with printing resolutions less than 100 nm and a depth of focus (DOF) greater than 1 nm are expected. Technology scaling is expected to support several IC generations down to possibly 0.03 nm.



Because extreme ultraviolet (EUV) photons are highly absorbed in most materials and gases, special reflective optics contained in a vacuum environment are required to produce imaging. In the late 1980s, Bell Laboratories, LLNL, SNL, and Japanese researchers performed early research using soft X-ray projection lithography. During the early and mid 1990s, research continued, and laboratory cameras were demonstrated. In 1996, DOE reduced funding for EUV work at the national labs and research within Bell Laboratories. With the support of Motorola, Inc., and Advanced Micro Devices, Inc. (AMD), Intel Corporation sponsored the formation of the EUV Limited Liability Corporation (EUVLLC) consortium. A Virtual National Laboratory (VNL), comprised of LLNL, Lawrence Berkeley National Laboratory (LBNL), and SNL, is working with the EUVLLC to continue EUV R&D work.

The EUVLLC lithography goals include:

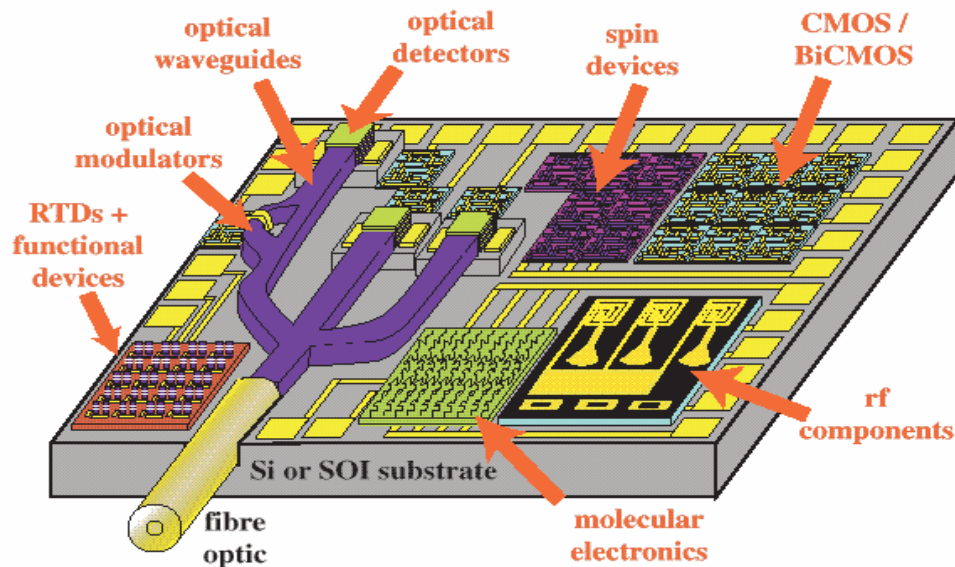
- An engineering test stand (ETS) in late 1999
- Stepper beta tools by 2001
- Pre-production and production tools by 2002 and 2004, respectively.

The initial lithography tool goals for the illuminator include using a continuous, recycling xenon gas jet laser plasma source and a 13.4-nm condenser delivering > 98-percent uniformity and < 2-percent nonuniformity illumination over a  $1.5 \times 26$  mm ring field with a partial coherence of 0.7. The production lithography tool targets a scanned field the size of  $26 \text{ mm} \times 52.5 \text{ mm}$  printed on 300-mm wafers using 150-mm and 300-mm reflective masks and 4:1 reflective reduction projection optics. Wafer and reticle-handling interfaces will support a 300-mm system in a contamination-free vacuum environment with a throughput of 40 wafers per hour. At the International Society for Optical Engineering (SPIE) symposium in March 1999, Cymer, Inc., announced the availability of a doubly ionized lithium dense plasma focus laser source producing 13.5-nm radiation, 30-PM bandwidth, 760 MJ per pulse, and a 200-Hz repetition rate that they claim has significant advantages over currently available EUV sources.

### DATA SHEET III-8.3. NANOTECHNOLOGY

<b>Developing Critical Technology Parameter</b>	Develop material, processing technologies, < 100-nm lithography, quantum and conventional devices, and device architectures for a next generation of information processing systems and subsystems with critical feature sizes well below 0.1 $\mu\text{m}$ . Improve speed, density, power, and functionality to achieve speeds 10 to 100 times faster than current systems, density by a factor of 5 to 100, and lower power by a factor of more than 50.
<b>Critical Materials</b>	Resist for 193-nm and soft X-ray lithography, elastomeric polydimethylsiloxane (PDMS) for soft lithographic replication.
<b>Unique Test, Production, Inspection Equipment</b>	Highly anisotropic reactive ion etching (RIE) system; scanned probe microscopies; atomic force microscope; nano-positioning devices; nanoprobe for diagnostics; auger spectroscopy; high-temperature X-ray; neutron-scattering techniques.
<b>Unique Software</b>	None identified.
<b>Technical Issues</b>	Designing, fabricating, and testing electronic devices with critical feature sizes well below 0.1 $\mu\text{m}$ ; real-time control of the nanostructure fabrication for future quantum device-based electronics; techniques to enable combining III-V quantum device and standard CMOS electronics; resist development for 193-nm and soft X-ray lithography; lithographic replicating techniques; molecular beam epitaxy (MBE) with in situ process control.
<b>Major Commercial Applications</b>	For the manipulation of materials and data at the atomic level for applications such as computer storage technology, single electron tunneling (SET) devices are predominantly aimed at high-density, low-power memory markets. Resonant tunneling diodes (RTDs) have demonstrated numerous applications, and potential markets include digital-to-analog converters (DACs), clock quantisers, shift registers, and ultralow power SRAM. The RTDs can be designed for much higher speeds than CMOS for DACs and so forth, typically in the speed range 10 to 100 GHz, or for much lower power than CMOS, such as the SRAM technology. Phase shifter/frequency translator based on serrodyne modulation of a nonlinear transmission line for integrated sensor applications using terahertz signals.
<b>Affordability</b>	In reference to Moore's Law, manufacturers state that CMOS production past 100-nm ground rules is inevitable, but DRAM producers are more concerned that economics may limit future DRAM generations even before 100 nm is reached. The major companies are predicting that Moore's Law will slow toward 2010, but the reduction in cost per function on the chip will continue at the same rate because of changes in systems design, including self-test and error-tolerant architectures and increased integration levels leading to the system on a chip. The most important driver for new technology is the ability to reduce the cost per function on a chip. Present limitations are cross-talk and the lack of a silicon light emitter to increase functionality. Eventually, RF and optical functions (optical interchip/intersystem and on-chip interconnects) will be integrated onto CMOS/BiCMOS <sup>2</sup> chips to reduce systems costs. MCMs having two- or three-chip solutions instead of a one-chip solution may be a less expensive approach over complete systems-on-a-chip. Figure 8.3-2 is an example of a future system-on-a-chip.

<sup>2</sup> BiCMOS technology is a combination of Bipolar and CMOS technology. CMOS technology offers less power dissipation, smaller noise margins, and higher packing density. Bipolar technology, on the other hand, ensures high switching and input/output (I/O) speed and good noise performance.



**Figure 8.3-2. Future System-on-a-Chip**

(Source: ESPRIT – Microelectronics Advanced Research Initiative Nanoelectronics Roadmap)

<http://www.cordis.lm/esprit/src/melari.htm>

## RATIONALE

Industrial-applicable nanofabrication techniques must be able to produce millions or billions of these small structures in a quick, reliable, and cost-effective way. These techniques must be able to connect these structures in a predefined manner. For this reason, parallel techniques, such as conventional circuit lithography techniques using mask alignment and pattern transfer, seem to be the only currently realistic way to fabricate circuits that are highly integrated. Serial techniques, such as scanning probe techniques or e-beam lithography, may be useful for mask making, or single component fabrication but do not supply adequate throughput for large-scale ICs. Nanotechnology seeks improved speed, density, power, and functionality beyond that achieved by simply scaling transistors.

Specific military applications of this technology have not been clearly defined. Indications are that this technology will produce extremely small, very fast computers, integrated sensor applications using terahertz signals, and lightweight compact communication equipment—all with low power consumption.

## WORLDWIDE TECHNOLOGY ASSESSMENT

Austria	•	Belgium	••	France	••	Germany	•••
Italy	••	Japan	••••	Netherlands	••	Sweden	••
Switzerland	•••	UK	••	United States	••••		

Legend: Extensive R&D •••• Significant R&D ••• Moderate R&D •• Limited R&D •

R&D is being carried out throughout the industrial world. Countries with large efforts include the United States, France, Germany, Japan, Switzerland, and the United Kingdom.

### DATA SHEET III-8.3. NEXT-GENERATION LITHOGRAPHY

<b>Developing Critical Technology Parameter</b>	For microelectronics, lithographic technologies for the generation and transfer of highly complex patterns below 100 nm and to extend resolutions to 50 nm, using proximity X-ray, e-beam projection, EBDW, and ion projection [see <i>E-Beam Stepper; Background; Lithographic Requirements (Table 8.3-2); and Scattering With Angular Limitation in Projection Electron-beam Lithography (SCALPEL)</i> ].
<b>Critical Materials</b>	Advanced resist systems (bi-layer, thin-layer imaging, chemically amplified); X-ray, charged beam materials; antireflective materials for X-ray, e-beam, ion beam.
<b>Unique Test, Production, Inspection Equipment</b>	e-beam, X-ray, ion beam exposure equipment; mask inspection equipment; scanning probe microscopy (SPM); scanning capacitance microscopy (SCM); wafer level defect recognition and analysis.
<b>Unique Software</b>	Defect recognition and analysis; OPC; SQC.
<b>Technical Issues</b>	Alignment and registration accuracy; minimum resolvable feature size; increased depth of focus; exposure source integrity; process-generated defects; mask inspection; mask defect repair; metrology equipment for critical dimension and overlay. Military requirements not being addressed by the commercial sector are FPAs with unique IR requirements for military electronics and sensors.
<b>Major Commercial Applications</b>	Lithography is used in the fabrication of all semiconductor devices, MEMS devices, and ICs.
<b>Affordability</b>	Not an issue.

#### RATIONALE

The lithography and micropattern transfer technologies used to fabricate semiconductor devices, MEMS devices, and ICs are the keys in determining their performance and in maintaining a strategic edge in a wide range of military sensors, EW devices, communications, C2, and offensive and defense weapon systems. Lithography is the enabling technology that has supported the IC industry for decades. New, advanced lithographic technologies are required to adhere to the advanced performance projections for IC devices in the 21<sup>st</sup> century.

#### WORLDWIDE TECHNOLOGY ASSESSMENT

China	•	France	•	Germany	••	Japan	••••
Netherlands	••	Russia	••	South Korea	••	Switzerland	•••
Taiwan	•	UK	••	United States	••••		

Legend: Extensive R&D •••• Significant R&D ••• Moderate R&D •• Limited R&D •

#### BACKGROUND

#### LITHOGRAPHIC REQUIREMENTS

Advanced technologies, such as X-ray and EBDW, have been used to fabricate functional semiconductor devices below 100 nm over small field sizes at low throughput. In addition, various technologies have been proposed and studies are underway to extend resolution to 50 nm. X-ray mask capability for 180-nm generation is in development. Overlay requirements are among the most difficult technical challenges in lithography. Overlay and CD improvements have not kept pace with resolution improvements. The estimates for overlay appear to plateau around 30 nm.

Table 8.3-2 lists projected advances in lithography and overlay. This will be inadequate for ground rules less than 100 nm. Overlay CD control over large field sizes continue to be a major concern for < 130-nm lithography. Advances in stage technologies, environmental controls, interferometers, and alignment systems will be needed for < 65 nm overlay. Continuous improvements in mask-making technology (mask writers, inspection, repair, and substrates) required to support the technical and manufacturing needs of optical lithography below 250 nm. Mask inspection requirements will become more aggressive as X-ray and e-beam lithography push to finer resolutions. In addition, significant improvements will be necessary for all nonoptical approaches, especially 1× proximity X-ray. Major process and materials development is required to achieve the tolerances and mechanical properties necessary in the unique substrates used in these advanced technologies. Key issues will be identifying and repairing defects and the ability to keep masks defect free in manufacturing.

**Table 8.3-2. Critical Level Lithography Requirements**  
(Source: SIA NTRS)

Year of Production	1999	2001	2003	2006	2009	2012
Technology Generation	180 nm	150 nm	130 nm	100 nm	70 nm	50 nm
<i>Product Application</i>						
DRAM (bits)	1G	2G	4G	16G	64G	256G
MPU (logic transistors/cm <sup>2</sup> )	6M	10M	18M	39M	84M	180M
ASIC (usable transistors/cm <sup>2</sup> )	14M	16M	24M	40M	64M	100M
<i>Minimum Feature Size</i>						
MPU Gates (Isolated lines)	140	120	100	70	50	35
DRAM (Dense lines)	180	150	130	100	70	50
Contacts	200	170	140	110	80	60
Gates (nm, 3 sigma)	14	12	10	7	5	4
Overlay (nm, mean + 3 sigma)	65	55	45	35	25	20
DRAM Chip Size (mm <sup>2</sup> )						
<i>Year 1</i>	400	480	560	790	1120	1580
<i>Year 2</i>	320	390	450	630	900	1300
<i>Year 3</i>	240	290	340	480	670	950
MPU Chip Size (mm <sup>2</sup> )						
<i>Year 1</i>	360	400	430	520	620	750
<i>Year 2</i>	290	240	260	310	370	450
<i>Year 3</i>	220	240	260	310	370	450

### ***SCATTERING WITH ANGULAR LIMITATION IN PROJECTION ELECTRON-BEAM LITHOGRAPHY (SCALPEL)***

In January 1999, Lucent Technologies, Inc., Applied Materials, Inc., and ASM Lithography Holding N.V. announced their intention to cooperate in accelerating the development of SCALPEL e-beam lithography. The ultimate goal of this effort is to commercialize SCALPEL technology as a production-worthy manufacturing tool for building future generations of silicon chips. Several of the world's leading semiconductor companies have also expressed interest in supporting this effort.

SCALPEL is emerging as a viable choice for producing lithography generations below the 180-nm critical dimension. It provides image resolution and fidelity beyond the reasonable diffraction limits of advanced UV optical lithography tools. Wafer throughput will be a major factor in determining which post-optical lithographic technology candidate will provide the best productivity per unit cost. The SIA NTRS illustrates the need for device productivity in the post-optical generations, with increasing wafer size and multiple "shrink generations." In evaluating new lithography approaches, throughput must be normalized to various initial and continuing costs of the tools, masks, resists, metrology techniques, and supporting infrastructure.

In the past, e-beam lithography lacked sufficient throughput to be economically viable for chip manufacturing. In contrast EBDW systems, SCALPEL is a projection imaging system, distinguished by its use of an electron-scattering contrast generation mechanism. Proponents expect SCALPEL to overcome the limitations of optical lithography and enable the migration of chip technology to the 50-nm generation and beyond. An e-beam has a wavelength many times shorter than that of the UV light source used in today's lithography tools and has already demonstrated capability to pattern images well below 100 nm. Electron optics designed for the SCALPEL approach can typically provide a 3-mm wide wafer-scale effective field in which an imaging subfield of 0.25-mm width can be dynamically deflected without mechanical stage motion to expose the 3-mm area. High throughput is enabled by associating mechanical-stage motion in conjunction with the unit area to cover the wafer.

### DATA SHEET III-8.3. OPTICAL METROLOGY (WAFER INSPECTION)

<b>Developing Critical Technology Parameter</b>	An important area in optical metrology is wafer/mask inspection. The required precision for critical dimensions is in the tens of nanometers for critical dimensions of 250 nm and below. This presents a fundamental challenge and requires research on several fronts. Two approaches to solve this challenge are vector beam imaging and near-field optics. Critical technology parameters are CD measurement precision (5 nm) and minimum detectable particle size (5 nm).
<b>Critical Materials</b>	Materials for ultrasharp metal tip fabrication (near-field optics); bulk material for polarization control and waveguide optics for polarization control.
<b>Unique Test, Production, Inspection Equipment</b>	Near-field optical systems (currently in production but techniques for enhanced sensitivity and resolution are in active development); vector beam imaging (in its infancy and needs considerable research investment); precision mechanical systems for scanning (important in both fields).
<b>Unique Software</b>	High-speed acquisition/processing of digital images.
<b>Technical Issues</b>	The determination and implementation of optimum vector field distribution in the object plane.
<b>Major Commercial Applications</b>	Semiconductor inspection; biological imaging.
<b>Affordability</b>	No near-field systems suitable for automated semiconductor inspection are currently available. Laboratory systems are \$1–2 K.

#### ***RATIONALE***

The use of silicon ICs pervades defense and commercial communication systems and military weapons systems. For ICs to continue to support the current requirements, they must become two to four times more dense in terms of computer power. As line widths and device sizes decrease, critical dimension measurement and particle detection become very critical.

#### ***WORLDWIDE TECHNOLOGY ASSESSMENT***

Canada	•	China	•	France	•	Germany	•••
Japan	•••	Netherlands	••	Russia	•	Sweden	•
Switzerland	•	UK	••	United States	•••		

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Legend:      Extensive R&D    ••••      Significant R&D    •••      Moderate R&D    ••      Limited R&D    •

### DATA SHEET III-8.3. SMALL CRITICAL-DIMENSION LITHOGRAPHY

<b>Developing Critical Technology Parameter</b>	In 10 to 20 years, the applications for microchips will require width or feature dimensions in the 5- to 10-nm range. Critical-dimension lithography technology requires the UV reflective and transmissive and catadioptric optics to address these wavelengths. Thin-film resist technology for 5- to 10-nm wavelengths and nonlinear material for super-resolved writing need to be developed. EUV light sources in the 5- to 10-nm range, in combination with near-field and nonlinear processing technology, will be required to accomplish this task.
<b>Critical Materials</b>	Thin-film resist material.
<b>Unique Test, Production, Inspection Equipment</b>	Mask overlay and alignment to better than 1 nm and defect (amplitude and phase metrology) measurements to 0.2 nm root mean square (rms) must be developed. Advanced aspheric polishing techniques and low-absorption refractory materials will be required. EUV phase-shifting interferometrics to characterize defects clearly is also required.
<b>Unique Software</b>	High-bandwidth schemes for maskless lithography and new considerations for optical design in the X-ray region will be required. Optical component phase measurement algorithms will be needed to characterize defects.
<b>Technical Issues</b>	Maskless systems must be developed to minimize the constraints of going to short wavelengths. High-power, short-wavelength sources are required to sustain high throughput. Metrology and testing of EUV systems are not currently sufficient to develop this technology fully, so improved capability with higher resolution is needed.
<b>Major Commercial Applications</b>	Many commercial applications (everything from computers to vehicle microprocessors) will benefit from this technology.
<b>Affordability</b>	In the 5- to 10-nm feature regime, one can fit three to five times as many chips on a given semiconductor substrate, thereby significantly reducing the cost of a given chip.

#### RATIONALE

This technology will inherently reduce the susceptibility of space electronics to radiation. The smaller features reduce the footprint of the electronics and allow many more algorithms and redundant circuits to fit on the same size chip that is currently used. Many military applications will benefit from this technology, especially since the overall cost will be reduced with the decrease in feature size (thus increasing the yield of chips per substrate). The small patterns are then used in combination with deposition, lift-off, and implantation technology to produce microcircuits on semiconductor chips.

#### WORLDWIDE TECHNOLOGY ASSESSMENT

Australia	•	Canada	••	China	•	France	••
Germany	•••	Iran	•	Israel	••	Japan	••••
Netherlands	•••	Russia	•	Singapore	••	South Korea	••
Sweden	•	Switzerland	•	Taiwan	••	UK	••
United States	••••						

Legend: Extensive R&D •••• Significant R&D ••• Moderate R&D •• Limited R&D •



### DATA SHEET III-8.3. SOFT LITHOGRAPHY FOR MICROELECTROMECHANICAL SYSTEMS (MEMS)

<b>Developing Critical Technology Parameter</b>	Lithographic technologies for the generation and transfer of more complex patterns, for micromechanical structures using EUVL that employ 10- to 14-nm soft X-ray photons; 193 nm UV lithography; proximity X-ray; e-beam projection; EBDW; ion projection; soft lithography for MEMS.
<b>Critical Materials</b>	Advanced resist systems (bi-layer, thin layer imaging, chemically amplified); X-ray, charged beam; EUV; optical materials; antireflective materials for optical, EUV, X-ray, e-beam, ion beam.
<b>Unique Test, Production, Inspection Equipment</b>	Optical, e-beam, X-ray, ion beam exposure equipment; front and backside mask alignment; mask inspection equipment; SPM; SCM; wafer level defect recognition and analysis; surface profiler; SEM.
<b>Unique Software</b>	Defect recognition and analysis; OPC; SQC.
<b>Technical Issues</b>	Alignment and registration accuracy; minimum resolvable feature size; increased depth of focus; exposure source integrity; process-generated defects; mask inspection; mask defect repair; metrology equipment for critical dimension and overlay; processes and equipment that will expedite the affordability and manufacturability of MEMS devices and systems.
<b>Major Commercial Applications</b>	Lithography is used in fabricating all MEMS devices. MEMS devices and macro systems will have broad commercial applications ranging from biomedical, diagnostics, automotive, robots, sensors, communications, and aerospace to printers.
<b>Affordability</b>	Lithographic fabrication processes for MEMS must be based on high volume and low cost.

#### ***RATIONALE***

Using an ever-expanding set of fabrication processes and materials, MEMS technology will provide parallel micro-assemblies, nonsilicon substrates, and fully 3-D structures, with the advantages of small size, low power, low mass, low cost, and high functionality. MEMS, when inserted into weapons systems ranging from smart munitions and sensors to high-maneuverability aircraft and identification friend or foe (IFF) systems, will bring to the military new levels of situational awareness, information to the soldier, and precision strike capability.

#### ***WORLDWIDE TECHNOLOGY ASSESSMENT***

Belgium	•	China	•	France	•	Germany	••
Hong Kong	•	Italy	•	Japan	••••	Netherlands	••
Russia	•	South Korea	•	Switzerland	••	Taiwan	•
UK	••	United States	••••				

Legend:      Extensive R&D    ••••      Significant R&D    •••      Moderate R&D    ••      Limited R&D    •

## **BACKGROUND**

### **SOFT LITHOGRAPHY**

Soft lithography refers to a set of low-cost techniques that will expedite the affordability and manufacturability of MEMS devices and systems. This approach relies on elastomeric elements to print organic inks (microcontact printing), to mold polymers (replica molding, micromolding in capillaries, and microtransfer molding), and to perform lithography in the near field. Fabrication of patterns and structures with feature sizes as small as 30 nm on both planar and nonplanar substrates has been demonstrated.

The soft lithography techniques use an elastomeric PDMS element with patterned relief on its surface to generate features. The PDMS elements are prepared by casting prepolymers against masters formed by conventional lithography. The methods can generate features on curved and reflective substrates and can pattern large areas rapidly—both metals and polymers. Distortion currently limits the methods to fabrication of single-layer structures. Near-term applications could include optical devices like polarizers, filters, wire grids, and surface acoustic wave (SAW) devices. Long-term goals include optical data storage systems, FPDs, and quantum devices. Soft lithography is not currently competitive with conventional lithography for multilayer fabrication where there are critical requirements for pattern regularity.

Soft lithography techniques include:

- **Nearfield phase shift lithography.** A PDMS element with micron-scale surface relief in conformal contact with a layer of photoresist modulates the intensity of light in the nearfield region. At phase boundaries, an intensity null results from a p-phase shift between recessed and unrecessed regions. Feature size range is 50 to 100 nm.
- **Replica molding.** A PDMS element is cast against a conventionally patterned master. Polyurethane is molded against the PDMS secondary master, thus replicating the original without damage. Feature size range is 230 nm.
- **Microcontact printing.** An alkanethiol solution is used to ink a patterned PDMS stamp. The stamp is brought into contact with the substrate, and the thiol ink is transferred and then forms a self-assembled monolayer that acts as a resist to etching. Feature size range is 300 nm.
- **Micromolding in capillaries.** Continuous channels are formed when a PDMS element is brought into conformal contact with a solid substrate. Capillary action fills the channels with a polymer precursor. The polymer is cured, and the stamp is removed. Feature size range is 1 nm.
- **Microtransfer molding.** A PDMS element is filled with a prepolymer or a ceramic precursor and placed on a substrate. The material is cured, and the stamp is removed. Feature size range is > 250-nm multilayer capability.
- **Solvent-assisted microcontact molding.** A PDMS element with a small amount of solvent spread over it is brought into contact with a polymer such as photoresist. The solvent swells the polymer, expanding it to fill the surface relief of the mold. Feature range is 60 nm.

### DATA SHEET III-8.3. TECHNOLOGY FOR MICROELECTROMECHANICAL SYSTEMS (MEMS)

<b>Developing Critical Technology Parameter</b>	MEMS technology enables the development of chemical, biological, and mechanical smart systems. MEMS is based on a manufacturing technology that has roots in micro-electronic fabrication technology. It merges the functions of computing, communication, and power together with sensing, actuating, and control to interact with the physical world.
<b>Critical Materials</b>	Thick photo resist; silicon substrates; SiC substrates; thin-film polysilicon; fluxless solder; piezoelectric thin films.
<b>Unique Test, Production, Inspection Equipment</b>	Front and backside mask alignment; surface profiler; plasma processing (etch and deposition); SEM; cluster tools; MBE; MOCVD.
<b>Unique Software</b>	CAD software for process, system, and packaging simulation.
<b>Technical Issues</b>	Tools, processes, and equipment that will expedite the affordability and manufacturability of MEMS devices and systems; new concepts in the integration of multiple devices to form dynamic systems (e.g., distributed plug-in sensors interconnected by wired or wireless networks sharing a common communication/power bus); new interface/packaging technologies for applications that require MEMS devices to be integrated intimately into a macro device (e.g., arrays of actuators or deformable gratings where systems require controlled access to selected physical parameters that are either being sensed or controlled); MEMS standards, particularly in packaging and bonding techniques.
<b>Major Commercial Applications</b>	MEMS devices and macro systems will have broad commercial applications ranging from biomedical, diagnostics, automotive, robots, sensors, communications, and aerospace to printers.
<b>Affordability</b>	MEMS devices will be a small fraction of the system's cost, size, and weight but will be critical to its operation, reliability, and affordability.

#### ***RATIONALE***

Using an ever-expanding set of fabrication processes and materials, MEMS technology will provide parallel microassemblies, nonsilicon substrates, and fully 3-D structures, with the advantages of small size, low power, low mass, low cost, and high functionality. New device concepts include the integration of micro devices with communication, control, computation and power components; miniature electromechanical signal processing elements (tuning elements, antennas, filters, and mixers); miniature optoelectromechanical devices; switches; fiber-optic interconnects and aligners; deformable gratings and tunable interferometers; force/motion balanced accelerometers and pressure sensors; atomic-resolution data storage; process control; and simultaneous, multiparameter sensing with monolithic sensor clusters.

Advanced device and process concepts exploit integrated, collocated actuators, sensors, and electronics to achieve new functionality, increased sensitivity, wider dynamic range, programmable characteristics, designed-in reliability, and self-testing. MEMS inserted into weapons systems, ranging from smart munitions and sensors to high-maneuverability aircraft and IFF systems, will bring to the military new levels of situational awareness, information to the soldier, and precision strike capability.

***WORLDWIDE TECHNOLOGY ASSESSMENT***

Belgium	• •	Canada	• •	China	• •	Czech Republic	•
France	• • •	Germany	• • •	Israel	•	Italy	•
Japan	• • • •	Netherlands	• • •	Russia	• •	South Korea	•
Switzerland	• • •	UK	• •	United States	• • • •		

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Legend:      Extensive R&D   • • • •      Significant R&D   • • •      Moderate R&D   • •      Limited R&D   •

## SECTION 8.4—MICROELECTRONICS

### *Highlights*

- The 1997 SIA NTRS predicts a very fast-paced growth of semiconductor technologies to the year 2012. Feature sizes of 50 to 100 nm and densities of 275 Gbits/chip for DRAMs and 1.4 Gbits/chip for microprocessors (108 transistors/cm<sup>2</sup>) are predicted.
- All the microelectronic characteristics projections are based on current techniques.
- Continual evolution of existing technologies [see Volume I of the Militarily Critical Technologies List (MCTL)] are shown here—from microprocessors, converters, memories, and gate arrays to the evolution of such emerging devices as neural networks, artificial intelligence (AI), optoelectronics, new materials, and advanced packaging.
- Microwave and other RF devices at the IC level are continuing to advance with higher frequency and power, following the rest of the technology but at a slower pace. SiGe, Si, GaAs, InP, and GaN are enhancing this effort.
- Advanced packaging technologies will increase the usability of density, speed, heat control, integration, and environmental technologies, which the extreme densities require.
- Radiation and temperature tolerance are improved by the application of new materials and fabrication.

### **OVERVIEW**

Semiconductor devices are pervasive in all military applications involving electronics. This section contains all the digital, analog, and hybrid (analog and digital combined) technology semiconductor devices at the IC level, PCB, or module level. Environmental technology, such as temperature and radiation tolerance, is included for these devices. Also covered are the MMICs and other RF devices operating at higher frequencies and power and not incorporating the emerging applications of SiC and GaN; IC design and testing involving the CAD of chips, PCBs, and modules; and specialized materials and materials techniques, such as SiC and SOI.

Virtually all space, air, ground, and ocean military systems involve microelectronics and are dependent on the advances in this technology to achieve their superior performance. Extremely low power, size, and weight allow advanced ICs to be used effectively in “wearable electronics,” in ground-vehicle electronics, and in ultrasmall reconnaissance aircraft.

Very-high-performance microprocessors of the future will be the main element in supercomputers made of networks of microprocessors. The extreme numbers of elements on a chip will allow an individual microprocessor to be a supercomputer itself, composed of multiple processors networked on the chip along with a very large memory and multiple I/O channels to form very powerful “systolic arrays.”

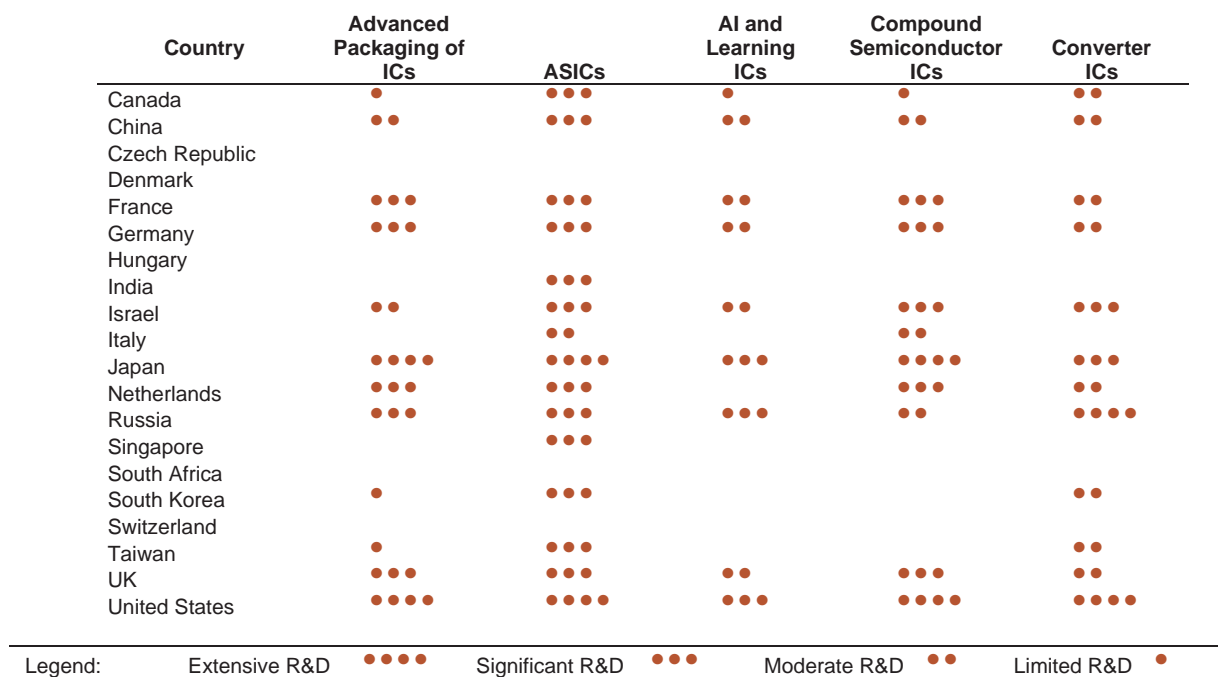
The integration of electronics and mechanical structures called MEMS will enable complete 3-axis inertial navigation “systems-on-a-chip,” including Global Positioning System (GPS) processing and interface, error modeling, drift compensation, and initialization.

### **RATIONALE**

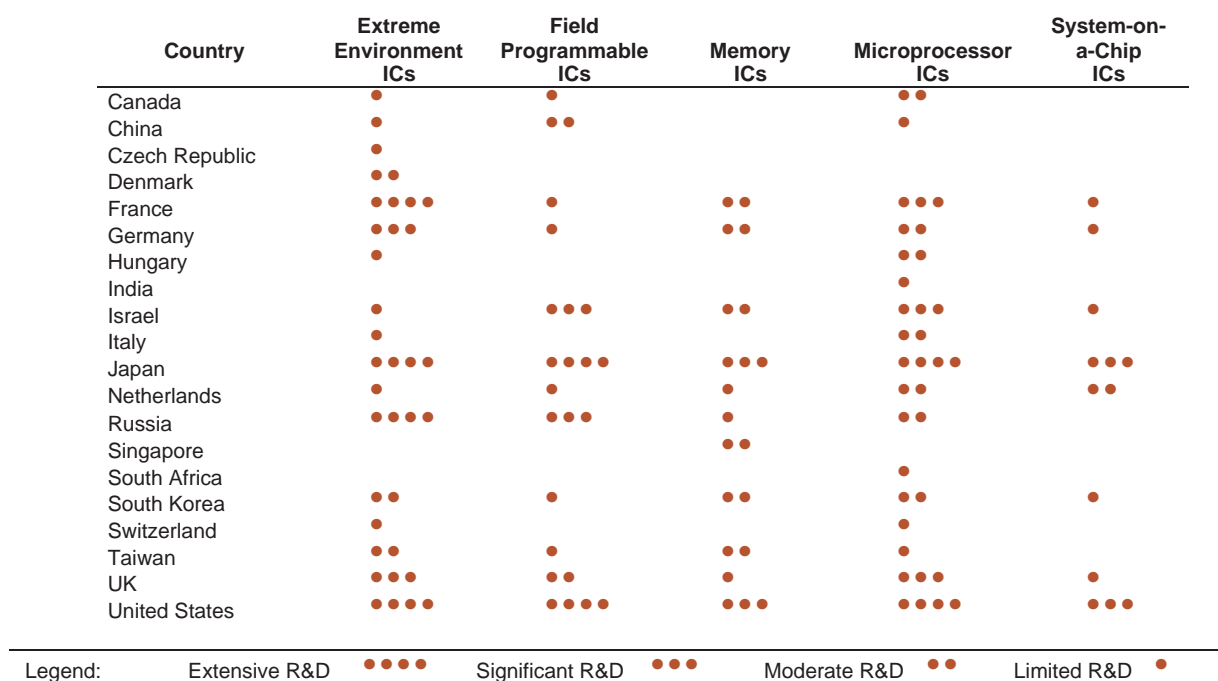
Microelectronic ICs are pervasive across all commercial and military systems and continue to improve the system performance. New IC technology is being inserted into new systems, and this continual improvement in electronics performance gives the United States a military advantage. High-performance electronics are used in strategic and tactical air, ground, underwater, and space applications. All smart weapons are totally dependent on ever-improving IC performance. The parameters of small size and low weight, low power, high reliability, and affordability give modern electronics their superiority.

The advanced technologies described in this section have some military benefit inherent in their characteristics. SOI and GaAs are inherently harder to total dose radiation, although smaller feature sizes are more susceptible to SEU. The use of diamond substrates and diamond coatings with better heat dissipation allow denser packaging and less susceptibility to shock and vibration.

**WORLDWIDE TECHNOLOGY ASSESSMENT** (see Figure 8.4-1)



**Figure 8.4-1. Microelectronics WTA Summary (1 of 2)**



**Figure 8.4-1. Microelectronics WTA Summary (2 of 2)**

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### DATA SHEET III-8.4. ADVANCED PACKAGING OF INTEGRATED CIRCUITS (ICs)

<b>Developing Critical Technology Parameter</b>	The advanced mobile military systems will require increased functionality per unit volume, and this need can be met only through innovative packaging and interconnect approaches [e.g., chip scale packaging (CSP) using flip chip technology]. Next-generation technologies must be developed for high-speed, mixed-signal circuits and increased level of integration, including embedded components and MEMS devices, to achieve functionality and miniaturization.
<b>Critical Materials</b>	High-density interconnect substrates [e.g., those using laminated multi-chip modules (MCM-Ls)], such as flex tape, are primarily multilayer plastic packages made up of copper and epoxy resin, ceramic multi-chip modules (MCM-Cs), deposited thin-film multi-chip modules (MCM-Ds), and built-up multilayer technology, such as MCM-L/D and MCM-C/D for wafer scale processing.  For micro-via technology, laser and photo-imageable dielectric layers and plasma etch technology are critical.
<b>Unique Test, Production, Inspection Equipment</b>	Burn-in and test fixtures and testers for MCMs or multi-chip assemblies (MCAs); thermal enclosure/interface systems for control of high temperature during testing; wafer level burn-in and testers for known good die (KGD); interconnects using copper; and optical microscope for solder reflow process control for bumping.
<b>Unique Software</b>	Design tools software; test and analysis software; process control software; thermal management software.
<b>Technical Issues</b>	Design tools and design experience; modeling and simulation for 3D packaging; heat dissipation, thermal mismatch, and size; reliability and thermal management of plastic and ceramic packages.
<b>Major Commercial Applications</b>	Solid-state memory; embedded processors for hand-held and portable products, desktop personal computers (PCs), notebooks, smart cards, camcorders, medical devices, analog/digital wireless applications, high performance computing (HPC) platforms, signal processors, communications, automotive, engine controls, and system-on-a-chip prototypes.
<b>Affordability</b>	In commercial markets, volume is the driver. Electronics-packaging and interconnect technology advances are leading to a small-die-size, ultrathin, lightweight, and low-cost package. CSP (flex tape and flip chip) technology represents only 25 percent of the total IC units assembled (leadframe packages). At present, advanced packaging is 3 times (1.5 cents vs. 0.5 cents/lead) the cost of thin small outline package (TSOP) and shrink small outline package (SSOP). However, with growing applications and existing manufacturing infrastructure, coupled with improvements in substrate materials and processes, it is expected that the prices will be as good or better. Smaller size, lower weight, and higher performance CSP and enhanced CSP packages are much more affordable and provide a better payoff to the system designer.

#### ***RATIONALE***

Multichip packages provide higher performance and increased miniaturization over individually packaged devices. Initial applications are in high reliability, high-speed modules, and compact functions. Since the inception of ICs, every improvement has required packaging innovations that do not degrade the IC's performance. Until the last several generations, these improvements have been achieved in a standard way.

Today's and future generations of ICs, with high-speed (gigahertz), high-heat dissipation (up to 50 W), and dense complex structures (gigabytes of memory and  $10^{12}$  logic elements), require new approaches and new

technologies. The large heat dissipation requires improved heat transmission from the active elements and the substrate. The higher temperature operation requires all the elements of the package to have similar or compensating differential expansion so the structure is not ruptured. Diamond films (and diamond substrates) have superior heat transmission. Copper runs have lower resistance and therefore generate less heat and conduct heat efficiently. Flip-chip and solder-bump connection techniques improve density and connectivity of larger MCMs.

All these technologies must not degrade the performance of high-speed chips at the subsystem interface layer. The MCM technology is a prototype for even denser chips that can incorporate multichips into a single chip as well as become the ultimate system-on-a-chip, which will include MEMS, optoelectronic functions, and hybrid analog and digital circuits.

#### ***WORLDWIDE TECHNOLOGY ASSESSMENT***

Canada	•	China	••	France	•••	Germany	••••	
Israel	••	Japan	••••	Netherlands	•••	Russia	••••	
South Korea	•	Taiwan	•	UK	•••	United States	•••••	
<hr/>								
Legend:	Extensive R&D	••••	Significant R&D	•••	Moderate R&D	••	Limited R&D	•

### **DATA SHEET III-8.4. APPLICATION-SPECIFIC INTEGRATED CIRCUITS (ASICs) [CUSTOM INTEGRATED CIRCUITS (ICs)]**

<b>Developing Critical Technology Parameter</b>	By 2012, 100 million gates/cm <sup>2</sup> at 1.5 GHz, with standard cells (microprocessor, memory, hybrid, I/O, A/D, and so forth) integrated into system (system-on-a-chip) ICs. Will perform almost all required applications and be competitive with GPICs. ASICs will be a large part of the future system ICs.
<b>Critical Materials</b>	Wafer flatness; minimum defects; uniformity for advanced ICs.
<b>Unique Test, Production, Inspection Equipment</b>	Lithography, epitaxy, deposition masks, and resists for high-density chips; high-speed testing equipment; chip probing.
<b>Unique Software</b>	Standard cell software simulation and modeling; high-level development language (HDL); common application environment (CAE); and automated test equipment (ATE).
<b>Technical Issues</b>	Quantity of production, size of chip in transistors, and speed. Need a military rapid prototyping tool development for unique military applications.
<b>Major Commercial Applications</b>	Pervasive to all commercial and military applications. Will compete with GPICs.
<b>Affordability</b>	Developed by commercial.

#### ***RATIONALE***

ASICs are “hardwired” (e.g., nonreprogrammable) logic devices that can contain complex logic, memory [DRAM, read-only memory (ROM), electrically erasable programmable read-only memory (EEPROM)], I/O circuits, and so forth—all on a dense chip with a large number of transistors ( $10^6$  to  $10^7$  in future). The technology is much like designing a general-purpose microprocessor or other special-purpose processors. Rather than use a programmable system in high-production electronics, a better approach is to fix the complete functionality of the chip (by using programmable devices) in an ASIC. The resulting chip is smaller, more economical, and more reliable than software-programmable devices.

ASICs are generally composites of “cells” transferred from other designs directly, such as logic for a whole microprocessor, a large DRAM and/or programmable read-only memory (PROM) [erasable programmable read-only memory (EPROM) or EEPROM], standard I/O structures for interfaces, timing circuits, and other whole functions desired. ASICs can be hybrid ICs (i.e., a mixture of analog, digital, and conversion functions).

In the future, a large percentage of mass-produced ICs will be ASICs. The ability to design a whole new unique structure using rapid prototyping design techniques (software or firmware) and HDLs can be done economically, fast, and correctly with minimum test time because the individual cells have been used many times and are therefore thoroughly tested and reliable.

ASICs allow the user to use ICs when ordering a standard device is impractical. The specified parameters indicate speed capabilities, which separate these devices from “run-of-the-mill” devices. Most ASICs have resulted from commercial development, but some have originated through military development.

ASICs can be produced in large quantities. They are reliable and are at the lowest cost per unit. Almost any electronic system house can create ASICs. The military can follow the same pattern using existing or specially designed commercial chips (e.g., COTS). The military can also replicate a design using MIL-SPEC designs, cells, and packaging to achieve a MIL-SPEC chip. Rad-hard chips can be created in the same fashion using the special materials and semiconductor structures required.

# ***WORLDWIDE TECHNOLOGY ASSESSMENT***

Canada	• • •	China	• • •	France	• • •	Germany	• • •
India	• • •	Israel	• • •	Italy	• •	Japan	• • • •
Netherlands	• • •	Russia	• • •	Singapore	• • •	South Korea	• • •
Taiwan	• • •	UK	• • •	United States	• • • •		

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Legend:	Extensive R&D	• • • •	Significant R&D	• • •	Moderate R&D	• •	Limited R&D	•
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### DATA SHEET III-8.4. ARTIFICIAL INTELLIGENCE (AI) AND LEARNING INTEGRATED CIRCUITS (ICs)

<b>Developing Critical Technology Parameter</b>	By 2017, 100 million neurons, with self-learning capability artificial neural networks (ANNs). Programmability of ICs for modeling and learning systems.
<b>Critical Materials</b>	Wafer flatness; minimum defects; uniformity for advanced ICs.
<b>Unique Test, Production, Inspection Equipment</b>	Lithography, epitaxy, deposition masks, and resists for high-density chips; high-speed testing equipment.
<b>Unique Software</b>	Training algorithms; simulation algorithms; simulation and modeling; HDL; CAE; ATE.
<b>Technical Issues</b>	Number of chip interconnects; optimization for broad range of electronic systems using massive parallelism; military system application (requires reconstituting learning/teaching/programming for specific application of AI and learning machines).
<b>Major Commercial Applications</b>	Robotics; nonlinear systems; modeling; control systems; central controller for very large systems; air traffic control; power plants; distribution networks; modeling of weather systems and other unpredictable systems.
<b>Affordability</b>	Cost of applying to specific military application.

#### ***RATIONALE***

High performance is required in complex control and decision-making systems (“expert or self-learning systems”), parallel processing systems, sonar signal discrimination, and speech and image recognition. Hardware and generic programming technology are available. Overlap between commercial and military applications could be large, allowing compatible usage.

Military use will be critical in battlefield control systems, decision-making systems, intelligence analysis, and so forth. However, the military will be using the commercial output for its technology base.

#### ***WORLDWIDE TECHNOLOGY ASSESSMENT***

Canada	•	China	••	France	••	Germany	••
Israel	••	Japan	•••	Russia	•••	UK	••
United States	•••						

Legend:	Extensive R&D	••••	Significant R&D	•••	Moderate R&D	••	Limited R&D	•
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### DATA SHEET III-8.4. COMPOUND SEMICONDUCTOR INTEGRATED CIRCUITS (ICs)

<b>Developing Critical Technology Parameter</b>	Denser ICs to achieve complex functions; matching packaging materials for uniform expansion at high temperatures.
<b>Critical Materials</b>	Compound materials (semiconductor, e.g., III/V and II/VI); GaAs epitaxial wafers; wafer flatness; minimum defects; uniformity for advanced ICs.
<b>Unique Test, Production, Inspection Equipment</b>	Lithography, epitaxy, deposition masks, and resists for high-density chips; high-speed testing equipment; chip probing modified for compound materials.
<b>Unique Software</b>	Simulation and modeling; HDL; CAE; ATE.
<b>Technical Issues</b>	Manufacturing difficulty; availability; difficulty in processing high-quality GaAs. Military must drive much of the development for radiation hardening, wide temperature range, and so forth.
<b>Major Commercial Applications</b>	Space electronics requiring radiation tolerance; jet engines for wide temperature range.
<b>Affordability</b>	One of the more expensive developments for the military but large payoff for both military and commercial areas.

#### ***RATIONALE***

Compound semiconductor ICs have attributes for high-radiation and/or high-temperature usage in a wide range of systems. They can be used to develop the integration of multiple-material ICs and can be used for all electronic equipment requiring unique properties for radiation hardening, wide temperature range, and so forth. Military and commercial areas share much basic research.

Compound semiconductor ICs have not reached their full potential for military applications because of modest volume and infrastructure needs that cannot be satisfied without compromising affordability. They have also not fully met their promise because of difficult materials and fabrication problems. These technologies have not had the large development funding or experience that the silicon ICs have had and are therefore running behind. However, the promise of special operational capabilities (rad-hard, high-temperature) have continued to propel these technologies forward. They will grow in capability as their properties become better understood and as the infrastructure is built to further the technology.

#### ***WORLDWIDE TECHNOLOGY ASSESSMENT***

Canada	•	China	••	France	•••	Germany	••••
Israel	•••	Italy	••	Japan	••••	Netherlands	•••
Russia	••	UK	•••	United States	••••		

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Legend:      Extensive R&D    ••••      Significant R&D    •••      Moderate R&D    ••      Limited R&D    •

### DATA SHEET III-8.4. CONVERTER INTEGRATED CIRCUITS (ICs)

<b>Developing Critical Technology Parameter</b>	100 MHz to 1 GHz samples/sec; 12- to 20-bit accuracies.
<b>Critical Materials</b>	Wafer flatness, minimum defects, and uniformity for advanced ICs.
<b>Unique Test, Production, Inspection Equipment</b>	Lithography, epitaxy, deposition masks, and resists for high-density chips; high-speed testing equipment.
<b>Unique Software</b>	Simulation and modeling; HDL; CAE; ATE.
<b>Technical Issues</b>	Digital accuracy (e.g., bit size); fast conversion; linearity; drift; cost of commercial products directly usable by military (COTS) if these products do not meet MIL-SPEC requirements.
<b>Major Commercial Applications</b>	Sensors, inertial guidance and navigation, control systems; display systems; medical systems.
<b>Affordability</b>	Military sometimes requires higher bit accuracies than commercial (e.g., 20- and 21-bit accuracies for ballistic missile aiming).

#### ***RATIONALE***

Converter ICs are critical components in all sensor-related systems (military and commercial). Fast, accurate converters are key and critical to real-time physical systems (e.g., sensor, inertial guidance and navigation, control systems, and so forth; display systems; digital mapping). These ICs are immediately available from commercial output. Overlap between commercial and military application could be large, allowing compatible usage.

#### ***WORLDWIDE TECHNOLOGY ASSESSMENT***

Canada	••	China	••	France	••	Germany	••
Israel	•••	Japan	•••	Netherlands	••	Russia	••••
South Korea	••	Taiwan	••	UK	••	United States	••••

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Legend:      Extensive R&D    ••••      Significant R&D    •••      Moderate R&D    ••      Limited R&D    •

### DATA SHEET III-8.4. EXTREME ENVIRONMENT INTEGRATED CIRCUITS (ICs)

<b>Developing Critical Technology Parameter</b>	Radiation > $5 \times 10^6$ rads (Si); total-dose-five merging devices; jet engine and automobile controls to 400 °C.
<b>Critical Materials</b>	Wafer flatness, thickness, defects, and uniformity for advanced ICs; ceramic, metal ceramic, diamond substrates, and diamond coatings; uniform expansion/contraction developed to mitigate thermal shock; SOI wafers; dielectric materials.
<b>Unique Test, Production, Inspection Equipment</b>	Dielectric isolation; SIMOX ion-implanter for deep implant on silicon-on-sapphire (SOS) and SOI; controlled doping; MBE; surface passivation; controlled radiation testing; reliability and failure analysis.
<b>Unique Software</b>	Computer modeling and simulation software; pre- and post-radiation modeling; SEU models; thermal analysis models; diagnostics for modeling of starting materials.
<b>Technical Issues</b>	Dielectrically isolated substrates; SOS or SOI technologies; field shields, diffused guard-bands, or hardened field oxides; use of diamond, GaAs, or SiC devices; device design base material (e.g., SiC or diamond vs. Si); thermal management; ceramic/metal substrates; additional radiation hardening for nuclear requirements.
<b>Major Commercial Applications</b>	All future large, low-power, high-speed, and high-density ICs as nanoelectronics are approached; commercial communications satellites; jet engines.
<b>Affordability</b>	Future commercial ICs in military systems will be more usable by COTS materials if military specifications are not too stringent. For military rad-hard devices, cost is an issue because of unique rad-hard-specific processes and low-volume requirements.

#### ***RATIONALE***

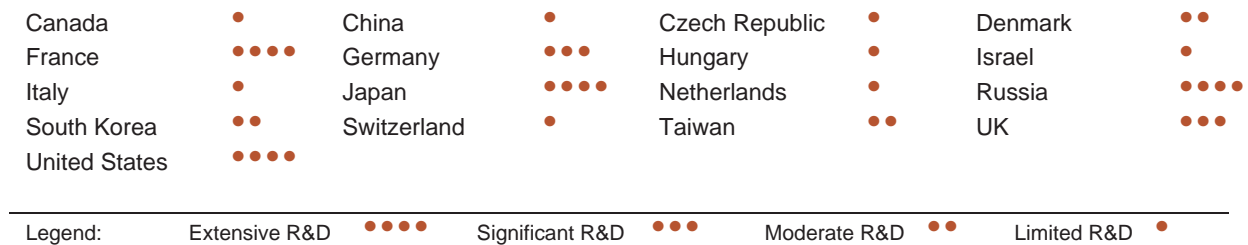
The ability of ICs to withstand the extreme environments of radiation, temperature, shock, and vibration improves the probability of reliable operation for all space-based military and nuclear systems. Generally, “mid-temperature range” has been accepted as an indication of improved long-term reliability for commercial systems, but the capability to operate at specified temperature extremes is critical in certain applications (e.g., missiles and nuclear systems) and may require special processing and packaging.

Commercial IC capabilities are continuously evolving to keep pace with the SIA NTRS. New technologies (e.g., SOI and SiGe wafers with Cu and low-k dielectric interconnects) are being implemented for low-power and high-speed complex ASICs, memory, and processors. However, the rad-hard-specific CMOS/SOI process and technologies are two to three generations behind the commercial IC device development and manufacturing.

As the COTS products become more common in the DoD environment, system designers can take advantage of the commercial capabilities and, by making modifications to the existing process and packaging techniques, develop systems to meet the radiation-tolerant applications for future military systems. However, for more stringent rad-hard and extreme-temperature devices, special circuit design/modeling, materials, and process development efforts are needed to keep pace with the commercial capabilities.



# ***WORLDWIDE TECHNOLOGY ASSESSMENT***



### DATA SHEET III-8.4. FIELD-PROGRAMMABLE INTEGRATED CIRCUITS (ICs)

<b>Developing Critical Technology Parameter</b>	Merging gate arrays and logic arrays into best architecture for field-programmable ICs; very large devices for all ranges of applications (especially ASICs); 1 million usable gates by 2012.
<b>Critical Materials</b>	Wafer flatness, minimum defects, and uniformity for advanced ICs.
<b>Unique Test, Production, Inspection Equipment</b>	Lithography, epitaxy, deposition masks, and resist for high-density chips; high-speed testing equipment.
<b>Unique Software</b>	Standard cell software simulation and modeling; HDL; CAE; ATE.
<b>Technical Issues</b>	Gates per chip; gate speed; throughput of custom architecture vs. custom ASIC; large military "software" development for field application.
<b>Major Commercial Applications</b>	Same as all future applications competing with GPICs.
<b>Affordability</b>	Commercially developed.

#### ***RATIONALE***

Field-programmable ICs will be used to prototype, modify, and upgrade military systems such as avionics, computers, radar, and guidance systems. Field-programmable gate array devices allow on-field changes to be made to existing firmware or software because of software changes, database changes, or additions to firmware or software. For military systems, a changed database could involve retargeting missiles, changing ballistics in fire control or missiles, or inserting new algorithms or programs to change the function of weapon processors.

A prime commercial use of field-programmable ICs is for programming a system temporarily for field test (e.g., Beta Site) before finalizing production design. These ICs can be used in the same way for military systems. Therefore, these devices can be compatible or interchangeable between commercial and military systems.

Field-programmable ICs are available from the commercial sector.

#### ***WORLDWIDE TECHNOLOGY ASSESSMENT***

Canada	•	China	••	France	•	Germany	•
Israel	•••	Japan	••••	Netherlands	•	Russia	••••
South Korea	•	Taiwan	•	UK	••	United States	••••
<hr/> Legend:      Extensive R&D    ••••      Significant R&D    •••      Moderate R&D    ••      Limited R&D    •							

### DATA SHEET III-8.4. MEMORY INTEGRATED CIRCUITS (ICs)

<b>Developing Critical Technology Parameter</b>	Very large (256 GB) and very fast (10 GHz) memory ICs (DRAM, SRAM, EPROM, EEPROM); large memory cells to be integrated into general-purpose microprocessors or ASICs by 2012.
<b>Critical Materials</b>	Wafer flatness, minimum defects, and uniformity for advanced ICs; GaAs, SiC/compound semiconductors.
<b>Unique Test, Production, Inspection Equipment</b>	Lithography, epitaxy, deposition masks, and resists for high-density chips; high-speed testing equipment.
<b>Unique Software</b>	Standard cell software; simulation and modeling; HDL; CAE; ATE.
<b>Technical Issues</b>	SRAMs—high storage capacity, high speeds and nonvolatile; compound semiconductor memory—high storage capacity, very high speeds, and rad hard; military usage developing GaAs, SiC, and other compound semiconductors for specific needs.
<b>Major Commercial Applications</b>	Pervasive to all commercial and military electronic systems.
<b>Affordability</b>	Commercial development will supply almost all military requirements if COTS products can be used or the commercial output can be directly converted to MIL-SPEC devices.

#### RATIONALE

Memory devices are critical components in almost all electronic systems; computer systems; equipment using avionics, missile control, and detection systems; air traffic control; guidance and navigation systems; communication systems; and complex electronic systems, subsystems, and products. It is expected that memory, like all ICs that follow “Moore’s Law,” will advance to the next generation every 2 to 3 years. The only constraint is the ability to invest large sums of money (approaching \$1 billion in the future) for the highly complex fabrication equipment that also must evolve in the same fashion. Certainly, gigabytes of memory on a chip will be available in several generations.

Further in the future, the role of memory in ASICs will begin to replace general-purpose microprocessors in many applications (not considering PCs, workstations, and so forth). Although ASICs for special-purpose functions in electronic systems are becoming very large and complex, they are easy to design and produce. So, the large bulk of future ICs will be for special-purpose functions with all firmware and databases stored in memory driven by a simple controller and complex interfaces.

#### WORLDWIDE TECHNOLOGY ASSESSMENT

France	••	Germany	••	Israel	••	Japan	•••
Netherlands	•	Russia	•	Singapore	••	South Korea	••
Taiwan	••	UK	•	United States	•••		

Legend:	Extensive R&D	••••	Significant R&D	•••	Moderate R&D	••	Limited R&D	•
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### DATA SHEET III-8.4. MICROPROCESSOR INTEGRATED CIRCUITS (ICs)

<b>Developing Critical Technology Parameter</b>	System-on-a-chip, including MEMS and optoelectronics; megabytes of SRAM on chips by 2012 for program and cache memory; 10-GHz speed by 2012; 1.4-B transistors/chip, including SRAM.
<b>Critical Materials</b>	Wafer flatness, minimum defects, and uniformity for advanced ICs; diamond substrates and coatings; efficient interconnects (such as copper).
<b>Unique Test, Production, Inspection Equipment</b>	Lithography, epitaxy, deposition masks, and resists for high-density chips; high-speed testing equipment.
<b>Unique Software</b>	Simulation and modeling for complex systems; HDL; CAE; ATE.
<b>Technical Issues</b>	Parallelism; reduced instruction set computers (RISCs) vs. complex instruction set computing (CISC) (architecture); density; yield in production; operating voltage and noise; heat dissipation; on-chip memory; performances of general-purpose microprocessors; I/O structure and memory access; price per function. In many cases, commercial output can be used directly by military (COTS).
<b>Major Commercial Applications</b>	Virtually all commercial applications; digital signal processors (DSPs); systolic arrays; massively parallel systems.
<b>Affordability</b>	Commercial (free) development allows direct use by military. Additional cost is incurred if military must meet MIL-SPEC requirements.

#### RATIONALE

Microprocessor ICs have become necessary and critical components in military and commercial systems. They are pervasive in all advanced military systems (e.g., radar, sonar, sensor, real-time signal- and image-processing systems). DSPs and other processors are also critical.

Immediately-available schedule of military insertion affects field timing. It includes digital filters and other digital implementations usually designed as ASICs.

#### WORLDWIDE TECHNOLOGY ASSESSMENT

Canada	••	China	•	France	•••	Germany	••
Hungary	••	India	•	Israel	•••	Italy	••
Japan	•••	Netherlands	••	Russia	••	South Africa	•
South Korea	••	Switzerland	•	Taiwan	•	UK	•••
United States	••••						

Legend:	Extensive R&D	••••	Significant R&D	•••	Moderate R&D	••	Limited R&D	•
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### DATA SHEET III-8.4. SYSTEM-ON-A-CHIP INTEGRATED CIRCUITS (ICs)

<b>Developing Critical Technology Parameter</b>	Integrate electronics, MEMS, optoelectronic, and hybrid circuits on a single chip, with all appropriate interfaces and A/D and D/A conversion.
<b>Critical Materials</b>	None identified, other than those noted on other data sheets.
<b>Unique Test, Production, Inspection Equipment</b>	Probe testing; total system testing; partial chip testing; ability to fabricate all these dissimilar technologies on a chip.
<b>Unique Software</b>	Simulation and modeling, including electronic, mechanical, optical; HDL.
<b>Technical Issues</b>	Ability to integrate different fabrication techniques on same chip; interfaces and heat control; applications to justify cost of development, design, and test; required signal integrity (grounding, shielding). MCM could be used.
<b>Major Commercial Applications</b>	Navigation and guidance; sensors; effectors; medical testing; miniature systems needing all characteristics.
<b>Affordability</b>	Design and fabrication cost will be high. Sufficient production will be required to justify cost.

#### ***RATIONALE***

Initial efforts will take advantage of extreme functional density to fabricate all electronics, including general-purpose computers (GPCs), DSPs, hybrid electronics, memory, and interface electronics for a large system function. Additional efforts will include integration of these same technologies, combined with MEMS, to develop gyros, accelerometers, medical sensors, and any miniature electromechanical functions. Electronic and optoelectronic integration will improve the development of computers, digital filters, and other signal-processing functions. The eventual goal will be to integrate all these functions into a single chip.

#### ***WORLDWIDE TECHNOLOGY ASSESSMENT***

France	•	Germany	•	Israel	•	Japan	•••
Netherlands	••	South Korea	•	UK	•	United States	•••
<hr/> Legend:      Extensive R&D    ••••      Significant R&D    •••      Moderate R&D    ••      Limited R&D    •							

This technology is in its infancy and has not yet taken advantage of the extreme functional size of even today's ICs. Some work has been done to put electronic interfaces on a MEMS accelerometer and gyroscope to create a workable function to interface with other navigation and guidance functions. Since MEMS are fabricated by IC equipment at micron-size features, the technology must be pushed to submicron features to be more compatible with today's dense chips.

Many sources are conducting exploratory R&D. Medical in-body sensors may drive the technology to new heights. Satellite navigation and guidance requiring the smallest size will also drive the technology.



## SECTION 8.5—NANOELECTRONICS

### *Highlights*

- All the attributes of microelectronics (see Section 8.4) are further enhanced by entering the nanoelectronics feature size range.
- EUV, X-ray, or ion-projection lithography will be used to break through the 100-nm barrier to achieve feature sizes down to 10 nm.
- The extreme density and speed of nanoelectronic devices will enable “supercomputers on a chip.” Integrated optical, mechanical, and electronic “systems on-a-chip,” such as complete inertial navigation systems, will be possible.
- Nanoelectronics will enable very small, low power, low cost, sophisticated space probes; microminiature biological probes for the human body; and battlefield surveillance using very small unmanned flying vehicles.

### **OVERVIEW**

Nanoelectronics can be broadly defined as those developing technologies required to push the size of devices down into the 100- to 10-nm (0.1 to 0.01  $\mu\text{m}$ ) region initially and then into the 10- to 1-nm region. Today’s advances in microelectronics technology continue to shrink the feature size of Si-based FETs and is projected to be 100 nm (0.1  $\mu\text{m}$ ) somewhere between 2003 and 2005 or earlier as per the SIA NTRS.

A nanometer is a billionth of a meter—about the size of two large atoms—approximately 10 atomic diameters. As this feature size shrinks below 100 nm, it will be more difficult and costly to fabricate these devices. Some investigators even question their functional effectiveness below 70 nm (by the year-2010 SIA NTRS) in ultradense ICs. A 25-nm dimension has been demonstrated, but many technical problems must be overcome before production can be achieved. In addition, packaging, interconnects, and heat will exacerbate the problem. In fact, these problems may be the initial stumbling block as current efforts approach the 100-nm region. Research has been ongoing for approximately the past 40 years to explore the alternatives for nanometer-scale electronic devices that can perform both as switches and amplifiers, just like today’s transistors for supercomputing applications. The operating principle for FET is the movement of mass electrons in bulk silicon. In the nanoelectronic world, atoms and molecules rule, and devices take advantage of quantum mechanical phenomenon including the discreteness of electrons.

Molecular electronics is a relatively new approach that would change the operating principle and the materials used in the electronic devices. It uses, primarily, covalently bonded molecular structures, electrically isolated from a bulk substrate. The molecules are naturally occurring nanometer-scale structures and can be made exactly the same by the millions and trillions easily and at low cost for the industrial scale nanostructures needed for the ultradense nanocomputers, where as it is difficult and expensive to fabricate millions and billions of nearly identical nanometer-scale structures in solids. Working at the molecular level could also lead to huge advances in optical communications and photonics, as well as ways to probe individual cells (speculative for now). In recent years, researchers have, for the first time, put together molecular electronics devices that measure only a few nanometers and are viable and inexpensive. Among the molecular switching device categories, the electric-field-controlled molecular devices and electromechanical molecular switching devices are promising because they descend from the solid-state microelectronics and nanoelectronic devices and show promise for super dense integration and super fast computing.

The breakthroughs required for extreme miniaturization fall into the following categories:

- **Device science.** Research on molecular electronics has been made feasible and important by the inventions of the new exciting methods called “mechanosynthesis” and “chemosynthesis.” Mechanosynthesis is the fabrication of nanostructures, molecule by molecule, using nanoprobe such as the scanning tunneling

microscope (STM), atomic force microscope (AFM), and the new MEMS chips that contain arrays of these STMs and AFMs.

Chemosynthesis is the fabrication of chemical “sub-assembly” of nanostructures using methods available from biochemistry, molecular genetics, and the organic synthesis of molecular electronic devices in individual organic molecules. It takes advantage of the driving force and speed of bulk chemical processes to make great quantities of nanometer-scale structures, such as molecular switches, nanowires, and self-assembled mono layers.

A new device science is required other than the bulk-effect FET. A potential new device might take advantage of quantum mechanical phenomenon that operate at these small feature sizes, including single electron actions. Two such classes are:

- *Solid-state quantum-effect and single electron devices.* This approach takes advantage of the long years of experience on semiconductor transistors.
- *Molecular electronic devices.* This approach is inherently nanometer in scale as it is molecular in nature. However, it requires new materials and processes.
- **Packaging.** Packaging for the nanometer-level devices will require extending the known approaches, and inventing completely new approaches, to overcome several difficult problems:
  - Heat dissipation reduction and control
  - Improved interconnects
  - Vertical integration of gate structures
  - 3-D packaging using vertical interconnects
  - New parallel architectures to optimize the chip layout.

Substrates and MCMs will have to use diamond coatings and metal ceramic technologies to achieve the required cooling. Copper runs (using Damascene and double Damascene techniques) and low-K insulators to achieve the desired speed and cooling will be required, as well as yet unknown techniques.

The kinds of challenges that need to be addressed are type of interconnection or linkage between molecules and small devices and solid substrate; electromigration and cross-talk problems in thin wires in ultradense structures; redundancy for error correction and reliability; heat dissipation; and the problem of how to arrange enormous numbers (between  $10^9$  and  $10^{12}$ ) of individual devices ultradensely and ultraprecisely on a surface or in a lattice structure. Also, the production of molecules that exhibit requisite electronic effect (e.g., Coulomb blockade) has to be shown.

## **RATIONALE**

For Moore’s Law<sup>2</sup> (double chip density and speed every 18 months) to continue in force, the feature size of semiconductor devices must continue to shrink below 0.10  $\mu\text{m}$  (100 nm) somewhere near the limit of optical lithography. These feature sizes are required for the destiny of chips to achieve the ultimate size required to build very large electronic “systems-on-a-chip.” These densities will also allow the integration of optical (both analog and digital), MEMS, and digital and analog electronics on a chip. The applications for chips of these sizes, both commercial and military, will be innumerable.

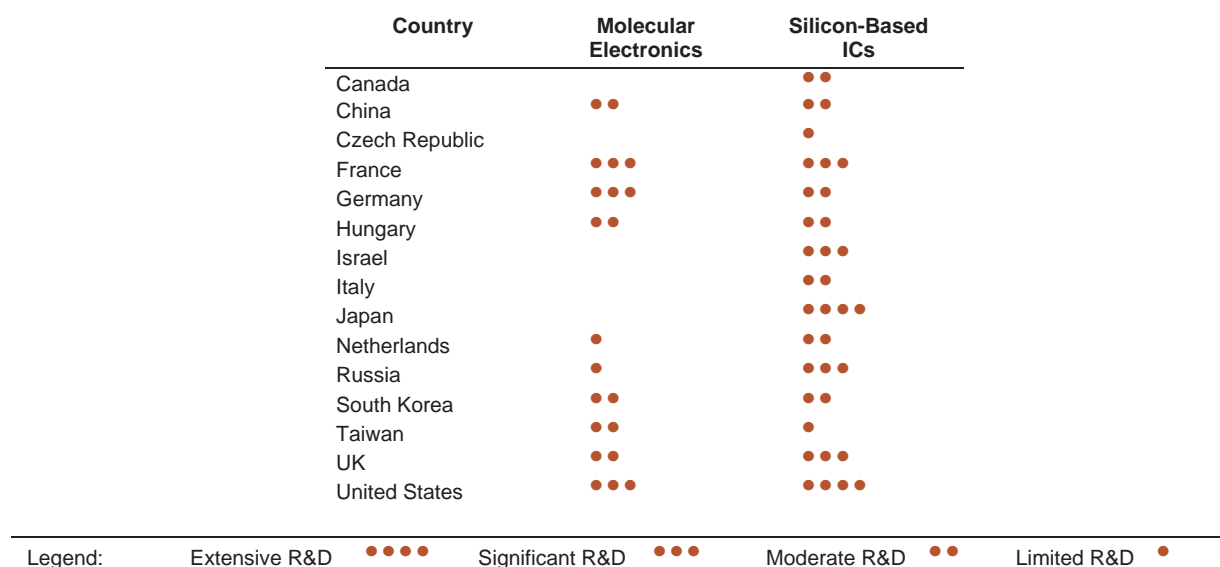
The commercial market will drive the requirements for these developments, but these developments will be directly applicable to future military requirements. The chips have some inherent capabilities to meet some military specifications (e.g., radiation tolerance, temperature range, shock, and vibration). Even if these advanced chips do not directly meet the required specifications, they are so small that they can be easily packaged to meet the requirements (e.g., shielding for radiation, heat sinks for temperature control, and shock and vibration mitigation).

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<sup>2</sup> Moore’s Law reflects the changes in IC technology but is used as the “Bible” by the Industry.



**WORLDWIDE TECHNOLOGY ASSESSMENT** (see Figure 8.5-1)



**Figure 8.5-1. Nanoelectronics WTA Summary**



**LIST OF TECHNOLOGY DATA SHEETS**  
**III-8.5. NANOELECTRONICS**

Molecular Electronics .....	III-8-69
Silicon-Based Integrated Circuits (ICs) .....	III-8-71



## DATA SHEET III-8.5. MOLECULAR ELECTRONICS

<b>Developing Critical Technology Parameter</b>	Molecular electronic technology (MET) includes devices relying on the electronic properties of molecules that may contain more than one electron and are not only “single” electron in nature. MET includes “single” electron (quantum cascade or quantum dot) or relies on electron spin. An example is the use of the position or spins of single electrons as the bistable logic gate in implementing nanometer-scale devices (below 10 nm). Microelectronic devices use silicon semiconductor current switching to accomplish bistable elements, whereas MET uses the location of single electrons or their spins as the switching element. Research at the University of Notre Dame in South Bend, Indiana, created nanometer-scale devices called quantum dot cellular automata as a logic gate. The Japanese have put effort into using not only the charges of electrons, but also their spins. The applications of these nanometer devices will ultimately improve greatly in performance, size, weight, power, heat dissipation, and perhaps radiation tolerance.
<b>Critical Materials</b>	Spin-controlled materials called magnetic semiconductors or multilayers of these materials have potential for these applications. Semiconductors and metals differ in the number of charge carriers involved. There are too many electrons in metals to be controlled. In semiconductors, the resistivity can be controlled by controlling the number of carriers, as in electrons or “holes.” Merging semiconductor and magnetic properties in a single material has been ongoing research for decades. II-VI alloys of magnetic and semiconductor materials are called diluted magnetic semiconductors (DMSs). Bulk forms of these II-VI DMS materials, thin films of III-V DMS (In,Mn)As, and a ferromagnetic DMS (Ga,NM)As are the various combinations.
<b>Unique Test, Production, Inspection Equipment</b>	A family of new test, production, and inspection (T, P, and I) equipment comparable to that used in microelectronics will have to be developed. It is not clear how many of the existing techniques can be transferred to nanoelectronics.
<b>Unique Software</b>	Since software is generally independent of hardware, chip tests and systems test for microelectronics might be adapted to nanoelectronics requirements. Testing and inspection during nanoelectronics production will require a completely new set of software. Application software generally should be interchangeable.
<b>Technical Issues</b>	The extremely large future cost for these nanoelectronic devices (in development, production, and application) must be weighed against the performance improvement that is expected—down to single-digit nanometer feature sizes. Further development is the only way to determine if the technology is feasible, practical, or even realizable. Achieving stable, reliable binary states for single electrons may be difficult. In theory and in the laboratory, it can be achieved; however, making it practical may not occur or may take excessive time, effort, and cost.
<b>Major Commercial Applications</b>	All the same applications used in microelectronics can be used in nanoelectronics. The major emphasis is on applications in which extremely small size, weight, power, and heat dissipation are essential, such as “wearable” electronics (both commercial and military); remote sensor systems (e.g., satellites, space probes, and biological in-body); ultrasmall, remotely piloted vehicles (e.g., microvehicles); and other smart vehicles (e.g., those used for underwater exploration).
<b>Affordability</b>	The initial discovery of the physics of silicon semiconductors has encompassed over 40 years of development and billions of dollars in expenditures. The development of MET has barely entered this kind of cycle. Certainly, initial discovery and analysis of molecular phenomenon has taken place during the last several decades, but the total thrust of development has been for silicon semiconductors. However, industry consensus is that silicon semiconductor technology cannot continue below 100–50 nm. All the technologies required for entering this regime—materials, lithography, deposition,

<b>Affordability (Continued)</b>	production equipment, testing methodology, equipment, and so forth—must be redeveloped. Certainly, the large, highly trained work force developed during the last 5 decades can collapse the timetable to achieve practical devices. So the final analysis is the cost to enter this technology. The cost to industry will be even higher because the two paths will inevitably be followed simultaneously—driving the present silicon technology to its ultimate limit and entering the new MET arena with all its uncertainties. History tells us that technologies tend to continue to proceed past their predicted limits. Surely, this will be the case with silicon technology since optical lithography has already exceeded recent predictions.
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## ***RATIONALE***

The commercial and military market will pressure electronics to continue to follow Moore's Law (double density every 18 months) and supply ever-higher performance. A challenge is whether the cost will be prohibitive and the users will be trained to accept a slower growth curve. However, the users can be expected to expand their system requirements, particularly with system-on-a-chip. The integration of digital and analog electronics, MEMS, and optoelectronics on a single chip will need ever smaller, lighter, lower power, higher performance, and rugged electronics. In the end, this will determine if the best in silicon technology is good enough to meet all market requirements.

The development of these devices cannot take advantage of all the microelectronic design, production, and application knowledge developed during the past few decades. The silicon technology of the past has become embedded in the culture, and this evolution has allowed tremendous advances to be achieved. However, MET will be a departure from all these existing technology and will require new physics, design, and production technology to be developed at great cost and over a long period of time. The question is, will industry will pay the price? Simpler departures in the past have not made the grade (two terminal devices comes to mind).

However, literature search shows that progress is being made in harnessing the principles of quantum mechanics to design and build molecular devices that can function well in nanoscale even after miniaturization of solid-state FETs has ceased to be feasible and cost effective. Before the nanofabrication methods become feasible, the industry may leverage the present microelectronics technology developments to pursue a hybrid solution for aggressive miniaturization by employing quantum effect and bulk devices. This may increase the logic density by as much as 100 or 1,000 times as that presently feasible.

## ***WORLDWIDE TECHNOLOGY ASSESSMENT***

China	••	EU (Consortium)	•••	France	•••	Germany	•••
Israel	••	Netherlands	•••	Russia	•	South Korea	••
Taiwan	••	UK	•••	United States	•••		

Legend:	Extensive R&D	••••	Significant R&D	•••	Moderate R&D	••	Limited R&D	•
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### DATA SHEET III-8.5. SILICON-BASED INTEGRATED CIRCUITS (ICs)

<b>Developing Critical Technology Parameter</b>	<p>Since industry has continued to invest in time and money in silicon-based semiconductors, it is locked into pushing the technology as far as it will go. It appears that the market will be satisfied for most of the next decade with predictable (some risk and large dollar investments) improvements in the ability of the underlying technologies to design and produce the required ICs into the less than 100-nm range.</p> <p>This is by no means a certainty since fundamental limits not approached to date will certainly at some point come into effect. Optical lithography may allow producing chips down to 50 nm in feature size, but this is not a certainty because of the need for extreme defect-free substrates and other fundamental problems.</p> <p>SIA NTRS projections for 2012 are:</p> <ul style="list-style-type: none"> <li>• Memory (DRAM) to <math>200 \times 10^{11}</math> bits/cm<sup>2</sup></li> <li>• Microprocessor (MPU) to <math>10^8</math> bits/cm<sup>2</sup>.</li> </ul> <p>Present capability is approaching 130 nm in production.</p>
<b>Critical Materials</b>	<p>Low-k dielectric deposition, copper chemical-mechanical planarization (CMP), and SiO<sub>2</sub> gates to achieve low delays (speed &gt; 2 GHz by 2012). For silicon nanodevices, defect-free and flat wafer, thin epitaxial Si or SiGe deposited films, new resist materials and light-sensitive coatings, low-k dielectric deposition, and interconnect materials (e.g., Cu) are critical. For Si nanoelectronic devices growth, and uniformity of SiO<sub>2</sub> to 5-nm thickness as a natural insulating barrier is important.</p> <p>Materials with low defect size, resists compatible with EUVL (see Section 8.3); heat sinking materials and techniques, such as diamond films, to allow 175 W per chip.</p>
<b>Unique Test, Production, Inspection Equipment</b>	<p>The existing T, P, and I equipment has kept pace with development to allow good ICs to be produced. For the next generation of ICs, this equipment is expected to continue to evolve. The T, P, and I parameters must always be better than the product to test properly beyond the product specifications. This means gigahertz frequencies and nanometer size. For scale-down field tests, development of lithography tools, masks, CMP tools, epitaxy and etch tools, and in-line automated defect inspection equipment with programs to analyze and categorize defects are needed for production. Also needed are ATE that has built-in test and advanced ATE that uses better probes and handling capabilities.</p> <p>The T, P, and I technology is pressed to the limits. A technique to help this situation is placing a permanent built-in test in the chip. Since future chips will have 10 power gates, these chips will have excess real estate available for redundancy, duplication, parallel data paths, stored test software and data, and so forth. This will be true for chip and chip-aided system tests.</p>
<b>Unique Software</b>	<p>New, extensive simulation and modeling capability; HDL, CAE, and ATE; defect monitor and failure analysis software programs for the in-line test. However, this should be an extension of the existing technology. The CAD software must be sophisticated to handle extremely large systems-on-a-chip, which entails analog, digital, optical, and mechanical engineering.</p>
<b>Technical Issues</b>	<p>The primary technical issue will remain the ultimate limit that will inevitably be reached where Moore's Law no longer applies. This will occur when the limits of optical lithography and attendant masking and resists are reached. In addition, the limit on current switching techniques as used in silicon-based technology will be reached when the physics involved no longer works. Some of the issues that can cause functional problems are shrinking feature size, quality, and uniformity of gate barrier to prevent tunneling; heat dissipation; vanishing bulk properties because of fewer dopant atoms; and</p>

<b>Technical Issues (Continued)</b>	<p>possibility of “avalanche breakdown” caused by high electric field. Interconnect and packaging for small devices may require new ways to avoid cross-talk and electromigration.</p> <p>Reducing power dissipation at these densities (50-nm feature size) will require reduction in voltage drain drain (VDD) to less than 0.5 V (possibly as low as 0.1 V).</p>
<b>Major Commercial Applications</b>	<p>All the major commercial applications stated in Section 8.4 apply here, except that the extremely large chips produced at the 50-nm feature size will be system-on-a-chip ASICs and very large computers on a chip (does not seem right to call them micro-processors anymore). These chips will likely be micro-optics-electro-mechanical systems (MOEMS) to take advantage of the large amount of space on the chip not needed for electronics alone. Since there will be a large availability of low cost yet capable chips at large feature size (e.g., in the 100 or less nanometer range), the use of these denser and more expensive chips may need to find their own market niches—in areas such as telecommunications, aircraft, and missiles using small inertial devices; supercomputing; optical communications; and photonics that are expected to be in large systems-on-a-chip.</p>
<b>Affordability</b>	<p>The SIA NTRS projects that the cost of new fabrications will increase to \$5 billion over the first decade of this century. The semiconductor industry has been meeting these costs as the new technology and the market demands. To date, the market has increased to absorb the costs and leave the industry profitable. New companies and consortiums have appeared to continue to provide the required output. However, as we approach the physical limits to the technology (projected in 2012 to 2014 at about 50 nm), the incremental costs will grow as elements of the technology become more difficult. Researchers project that to go beyond 50-nm device feature size, the Si FETs may be too expensive and inefficient—and thus unaffordable.</p> <p>At this point, the industry must shift to a new technology (“the new paradigm”) to continue the improvement in the product. The previous data sheet, Molecular Electronics, describes this new technology. It is not certain how the industry will absorb the costs of a new technology while in the midst of the most expensive part of the old technology. Since the market will not wait, the two technologies (old and new) must be pursued simultaneously so the transition is seamless.</p>

## ***RATIONALE***

The SIA NTRS “predicts” continual growth to the year 2014, following Moore’s Law (double density every 18 months). To continue the march of aggressive miniaturization per Moore’s Law and fabricate nanoscale (70 nm to > 5 nm) devices, optical lithography as we know it today will have reached its physical limit by year 2005 and will require new generation of lithography tools/technology to cross the barrier. Next-generation lithography (NGL) technologies, such as EUV using soft X-rays (being developed by an Intel consortium) and SCALPEL using electron-beam lithography (being developed by a Lucent consortium), are the prime considerations by SEMATECH/SIA member company experts. IBM’s candidate—X-ray lithography—is also in the race. The future cost of new facility using such new tools could run as high as \$3 to \$5 billion, excluding the cost of development.

Shrinking microelectronics have driven the exponential growth of Silicon Valley, but that growth will stop unless nanoscale computer chips can be fabricated. To continue this trend of miniaturization, the SIA NTRS projects that feature size to shrink to 100 nm by year 2005 (memory) and allows Moore’s Law to be in force. Researchers have projected that semiconductor transistors beyond 100 nm may not function as well. The problem is that dominant technology used to make chips. Optical lithography uses light whose wavelength may be too large to do the job. However, it has been shown recently that using phase shift masks and Numeri software techniques may extend optical lithography to 70 nm.

Major semiconductor manufacturers and tool builders—mostly in partnerships in United States, Europe, and Japan—are developing the alternatives (i.e., EUV, SCALPEL, and X-ray) being considered to surmount this barrier. These developments, coupled with interconnect materials and technologies, will also allow the fabrication of “system-on-a-chip,” which would integrate mixed signal devices and MEMS on the same chip. These lightweight, low-power, less costly, highly dense, and high-speed devices have tremendous applications in the commercial, space, and defense areas.



***WORLDWIDE TECHNOLOGY ASSESSMENT***

Canada	• •	China	• •	Czech Republic	•	France	• • •
Germany	• • •	India	• •	Israel	• • •	Italy	• •
Japan	• • • •	Netherlands	• • •	Russia	• • •	South Korea	• •
Taiwan	• •	UK	• • •	United States	• • • •		

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Legend:      Extensive R&D    • • • •      Significant R&D    • • •      Moderate R&D    • •      Limited R&D    •